CHERITech'26
CONFERENCE

CHERI

CHERIfication of DMA Engines

12-13 Nov 2026
Munich, DE

Ben Fletcher
IP Director @ Codasip
Working Group Lead @ CHERI Alliance



Located at semi | SEMICON EUROPA

Agenda

- Why CHERI-fy a DMA engine?
- EXAMPLE: Basic DMA walk-through
- EXAMPLE: Descriptor based DMA walk-through
- Putting this into practice

Why CHERI-fy a DMA Engine?



Why CHERI-fy a DMA engine?

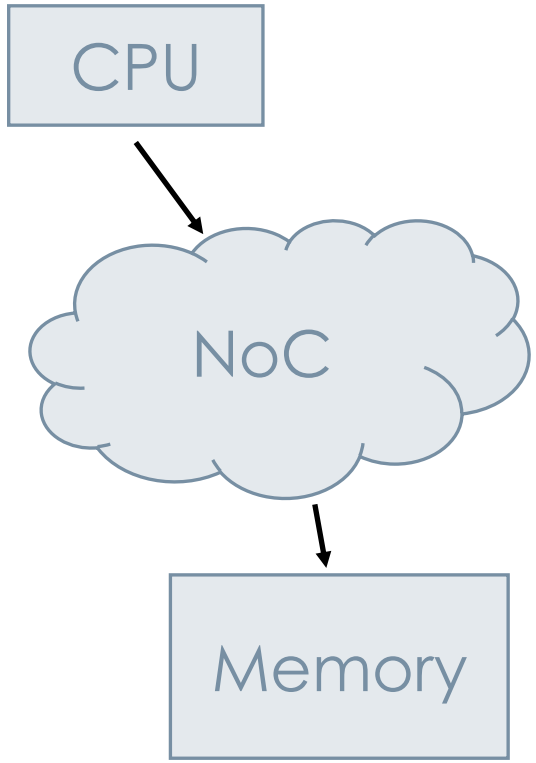
- A DMA engine is hardware that moves data between devices and memory autonomously.
  - Freeing the CPU from data-copying work.
- Building a system with CHERI is intended to improve memory safety.
- A non-CHERI-aware DMA engine is a capability-bypassing backdoor into memory.
  - Potentially reducing memory safety.

EXAMPLE: Basic DMA walkthrough



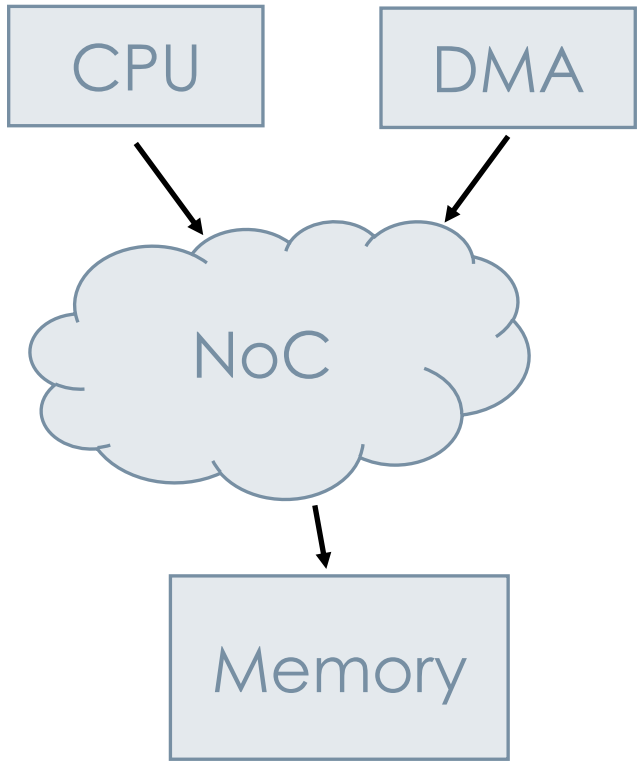
What does a regular DMA engine do?

- In a simple system a CPU might be connected to Memory via a NoC.
  - CPU can read and write data in memory.
  - CPU can be used to move quantities of data around memory.
  - However, this may not be an efficient use of resources.



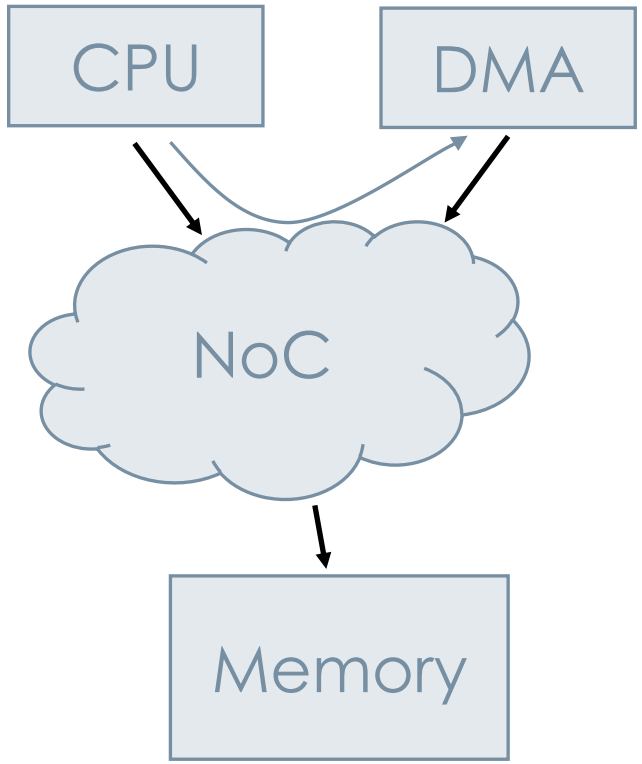
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- A DMA engine can be added to the system.
  - CPU can then delegate moving data around to the DMA engine.



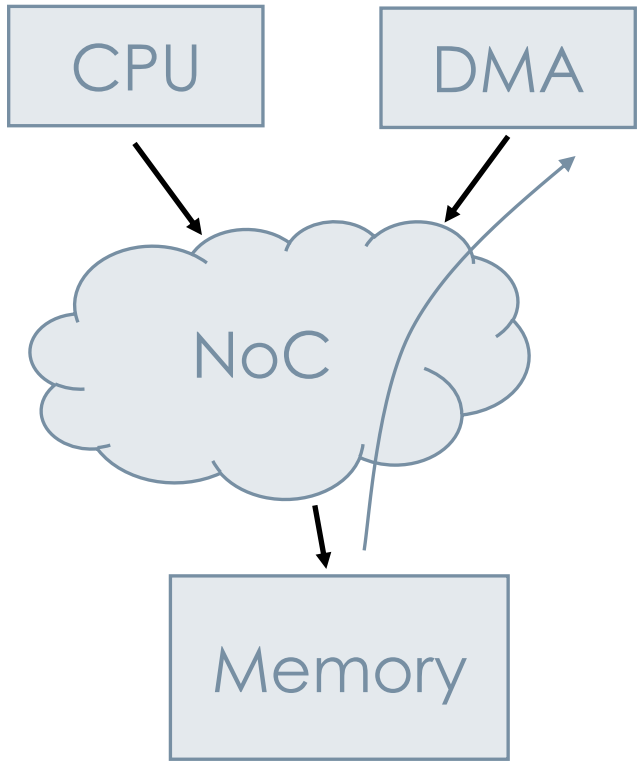
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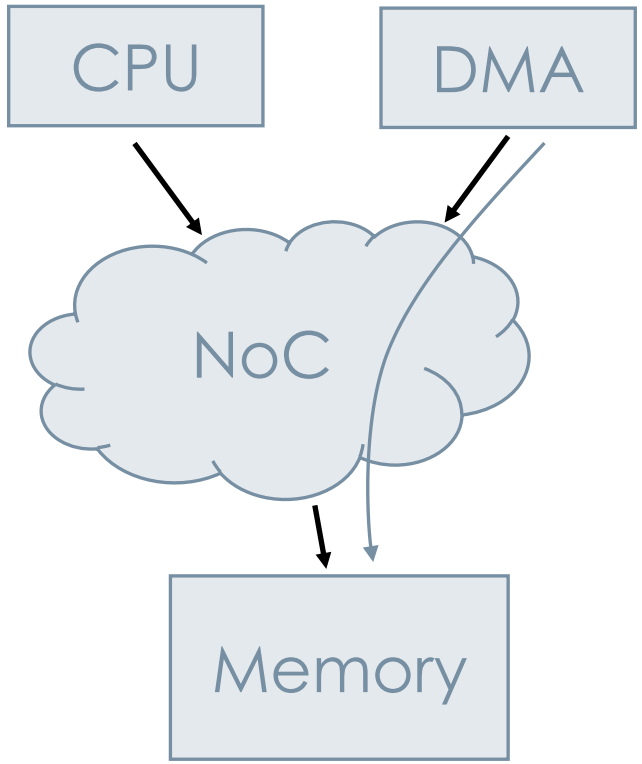
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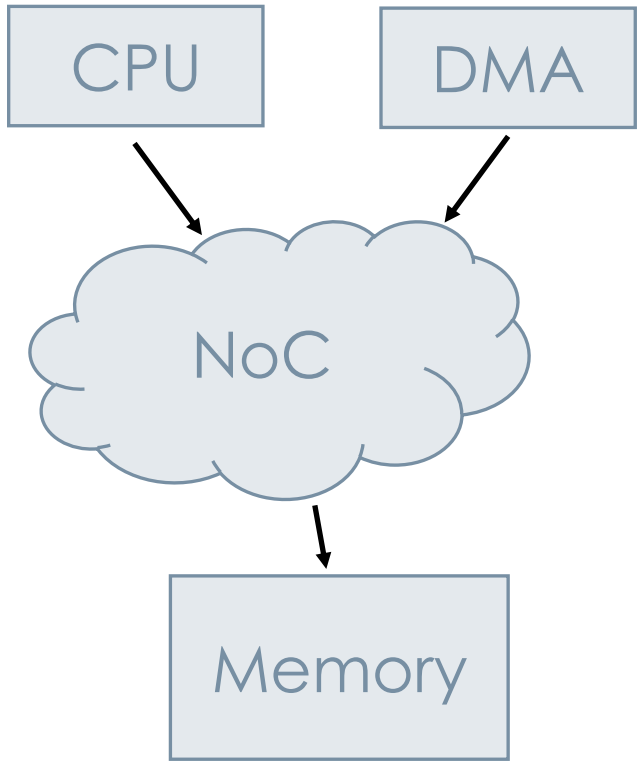
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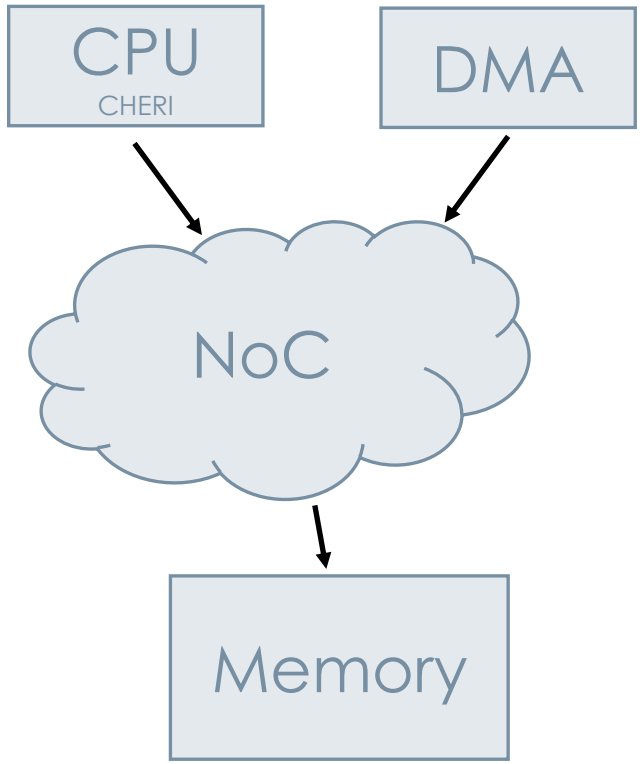
What does a regular DMA engine do?

- CPU writes information about the task to the DMA engine.
- DMA engine reads the data…
- …and writes it to the new location.
- The DMA engine is typically optimized to do this type of task quickly and efficiently.
- The CPU is freed up to do other things.



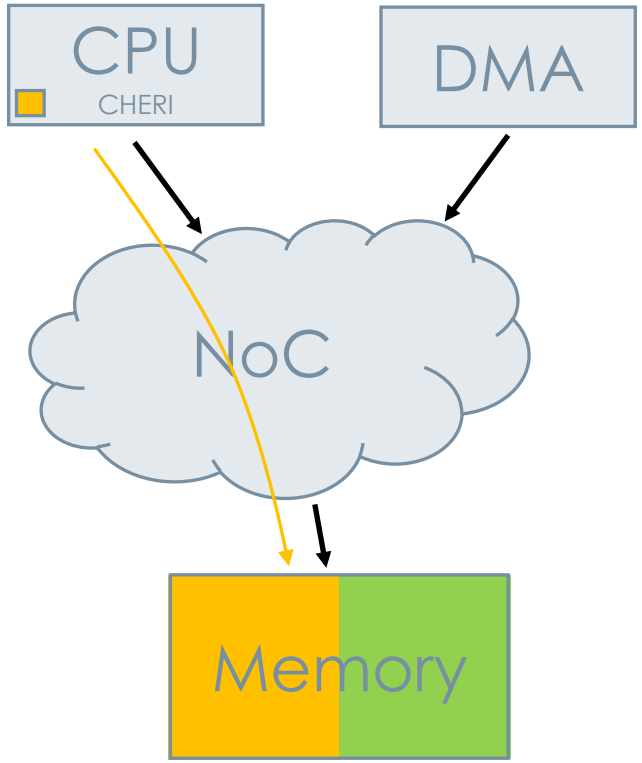
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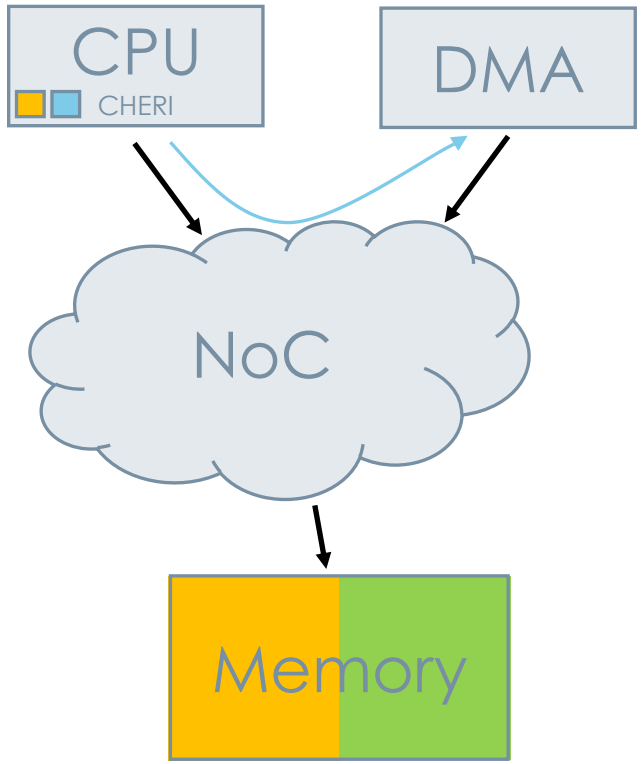
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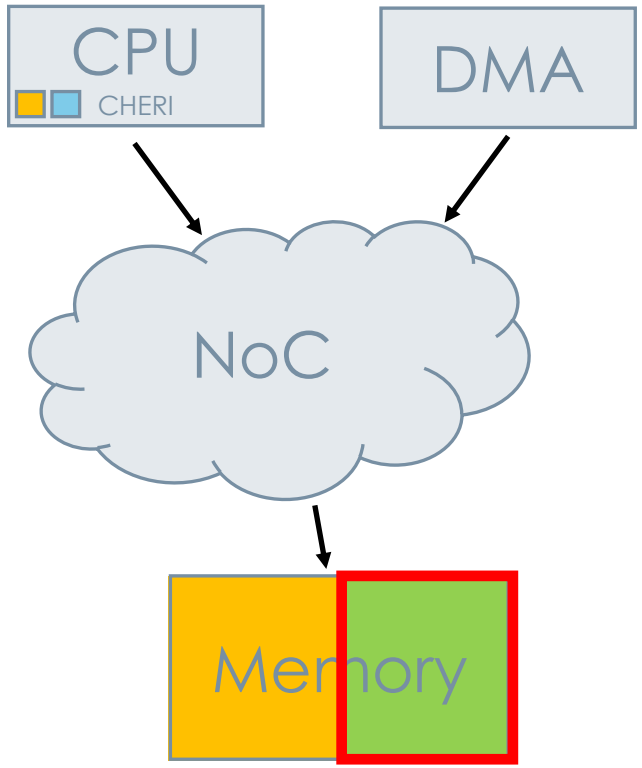
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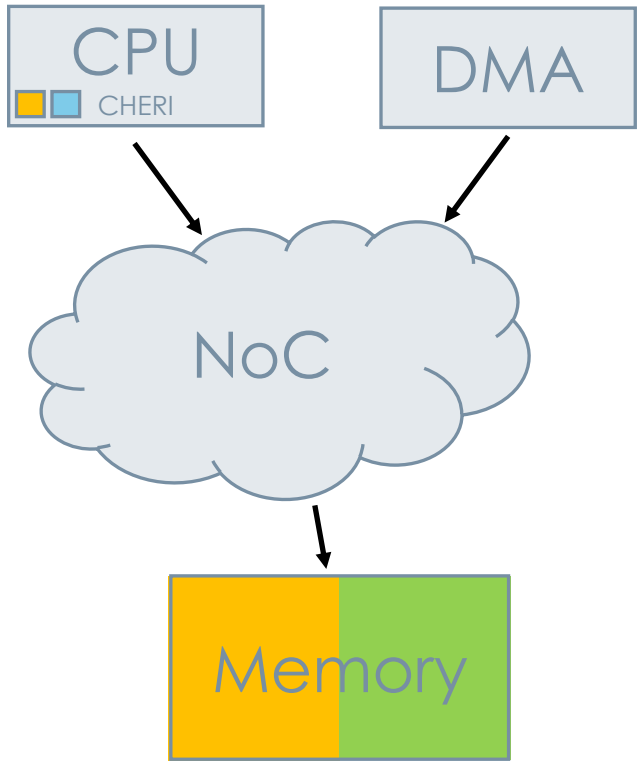
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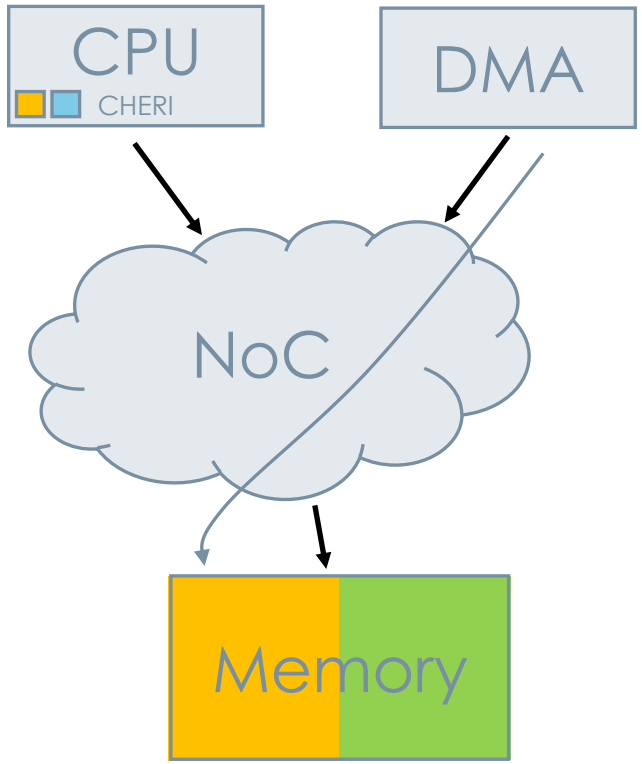
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- The non-CHERI-fied DMA engine does not need capabilities to provide authorization.



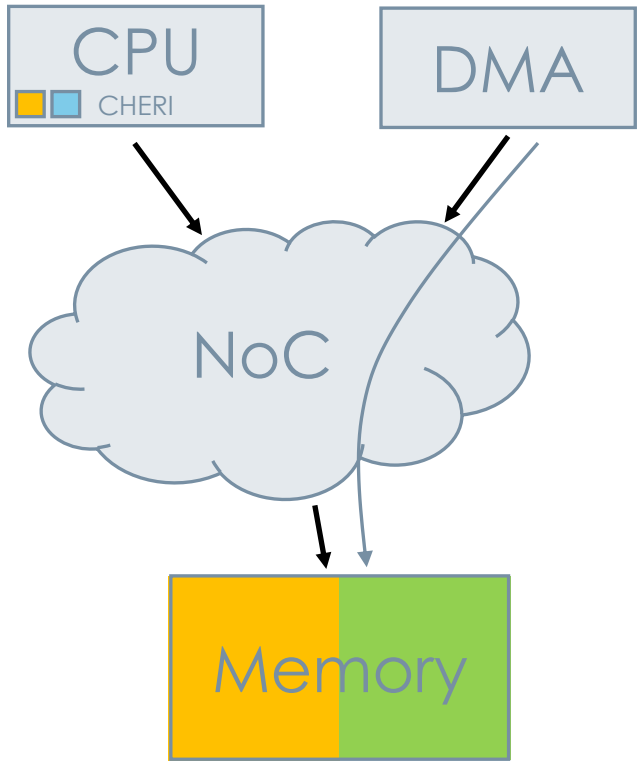
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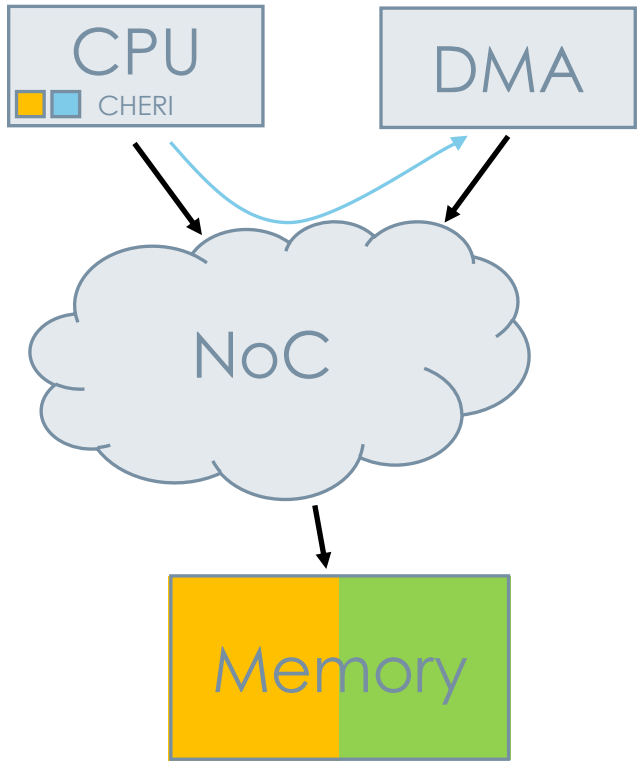
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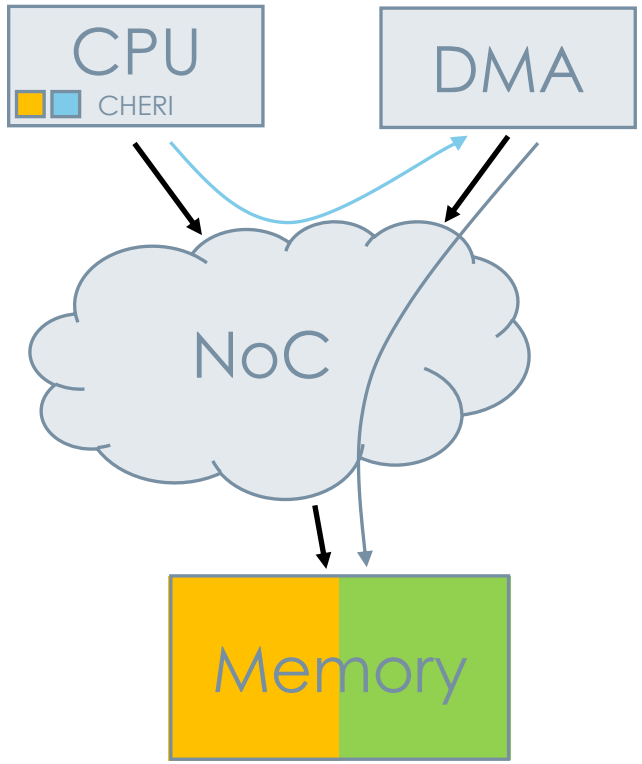
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- Any bus manager that can access the DMA engine…



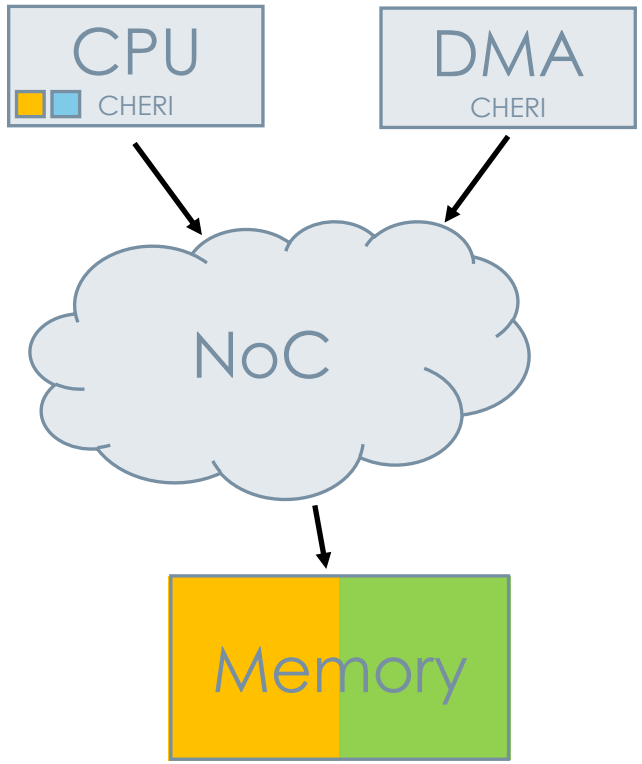
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- Any bus manager that can access the DMA engine…
- …can therefore get the DMA engine to provide access to memory without authorization.



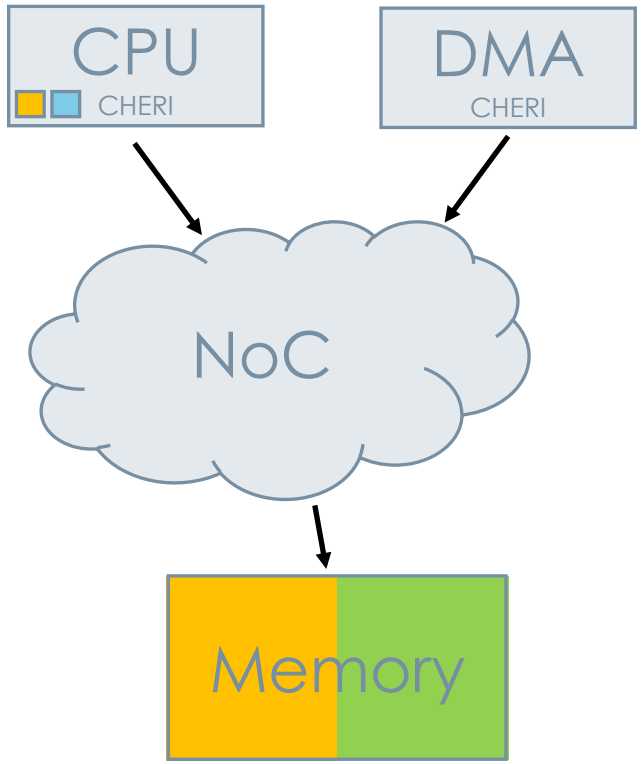
CHERI DMA

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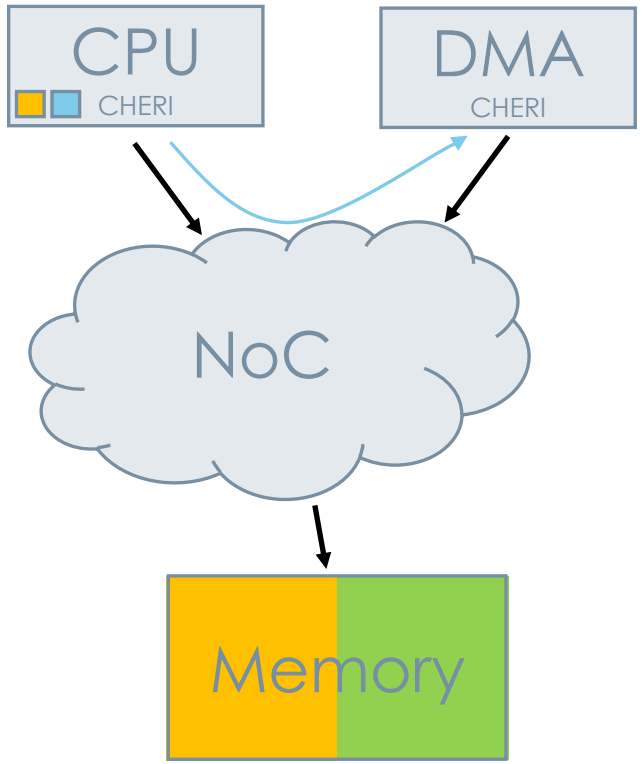
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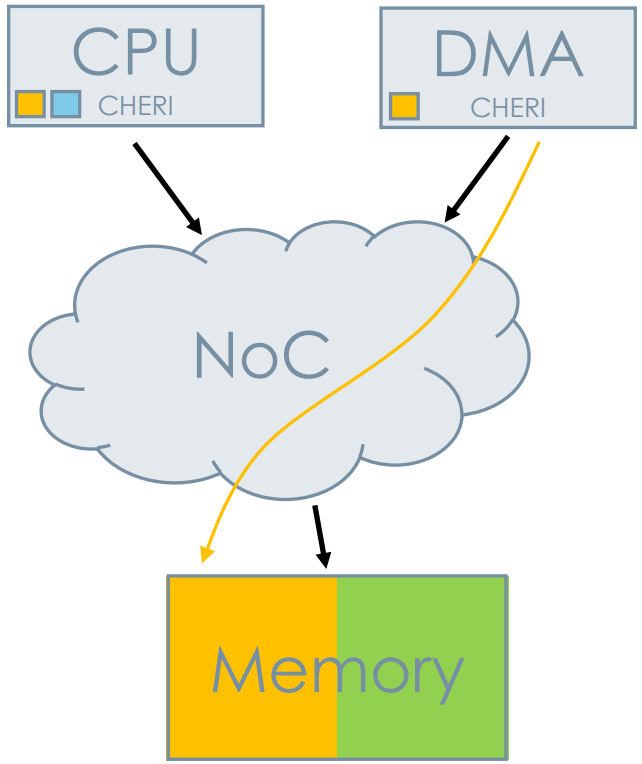
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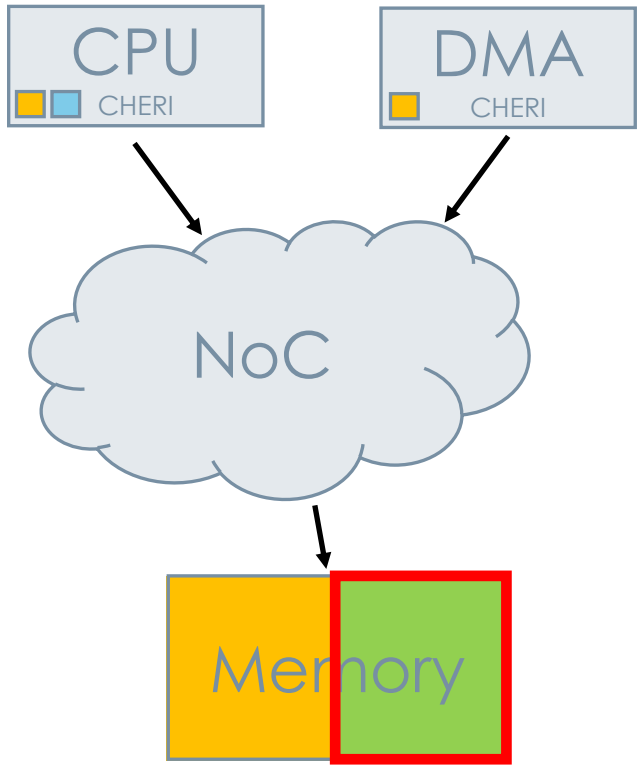
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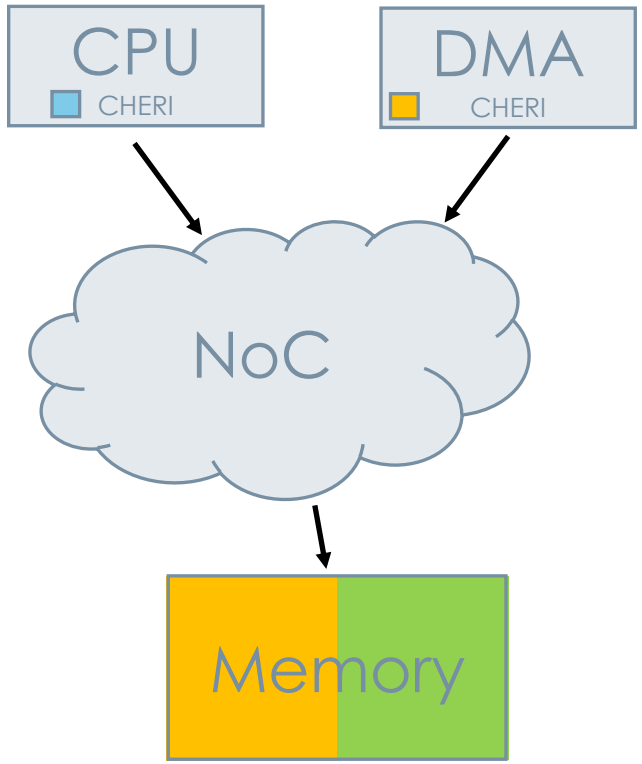
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- The DMA engine can no longer access arbitrary data in memory.



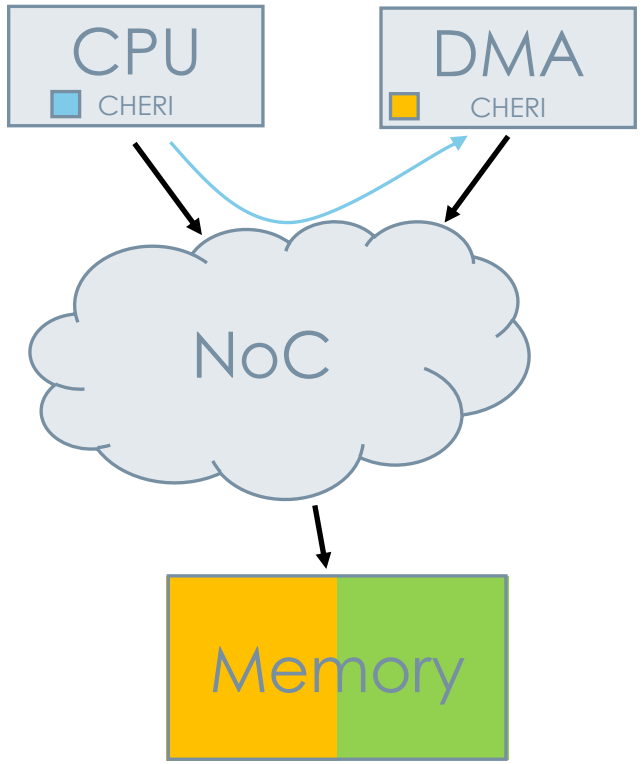
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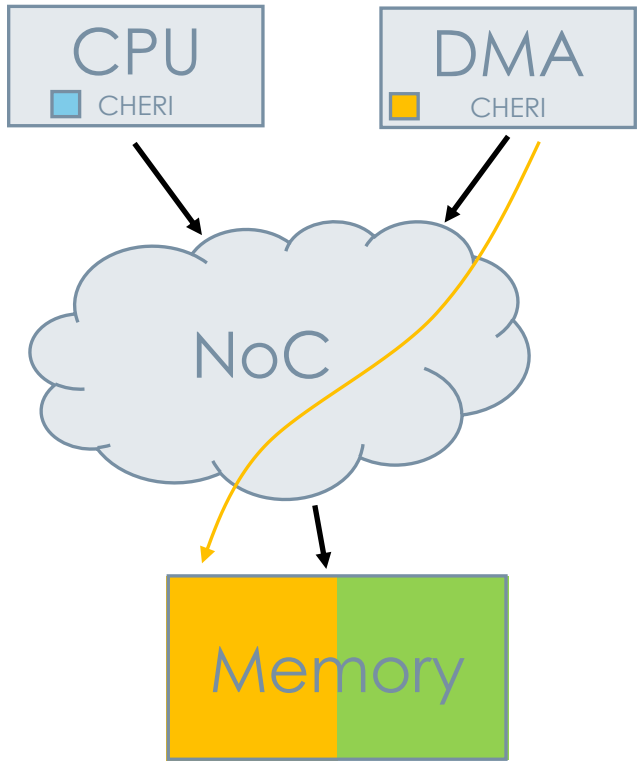
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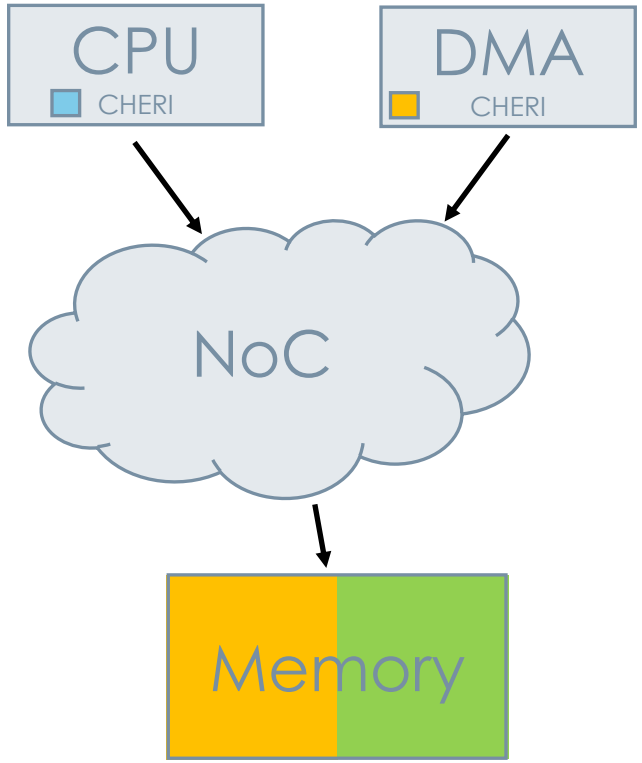
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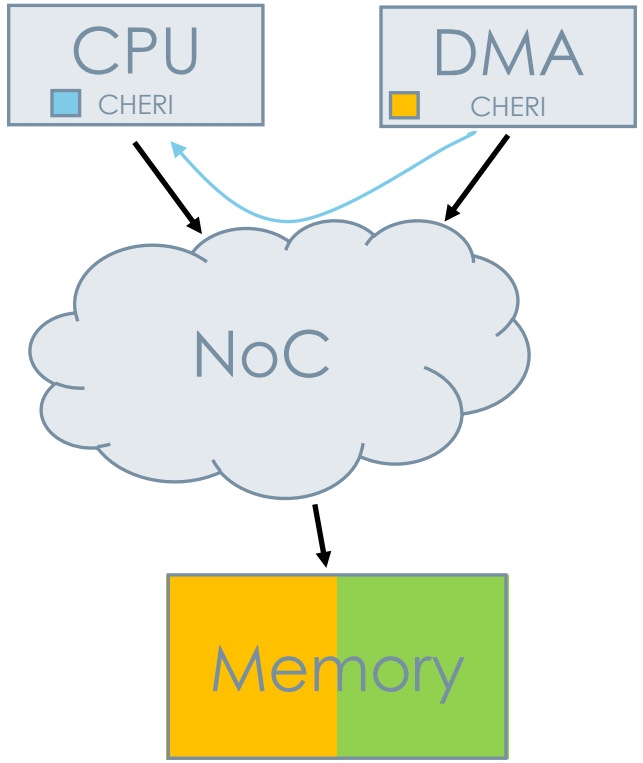
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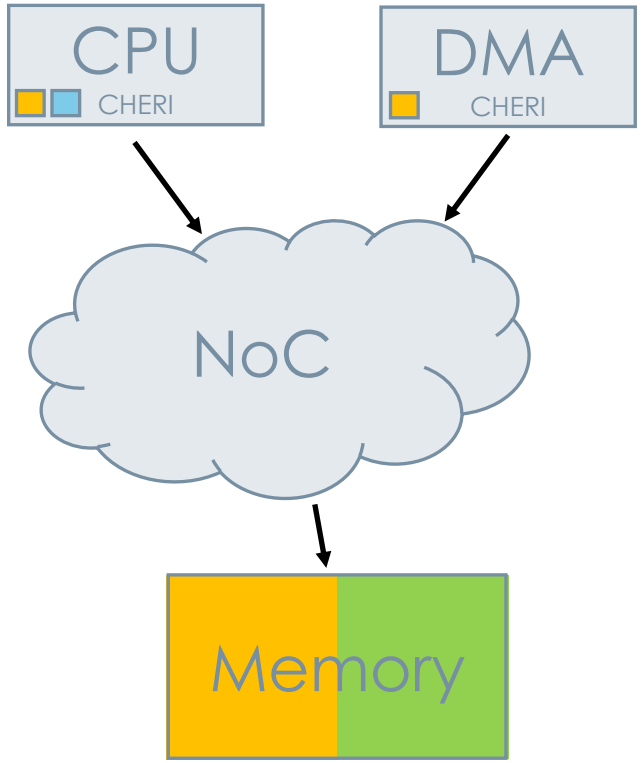
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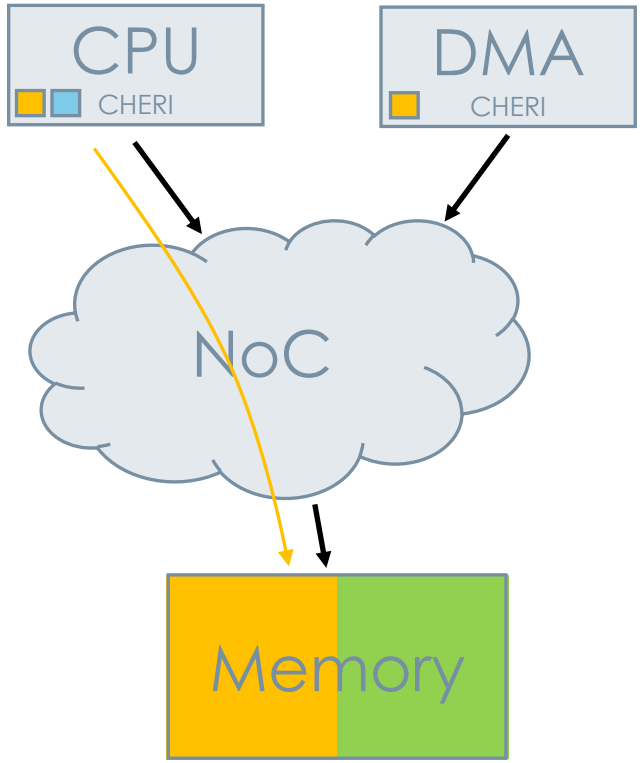
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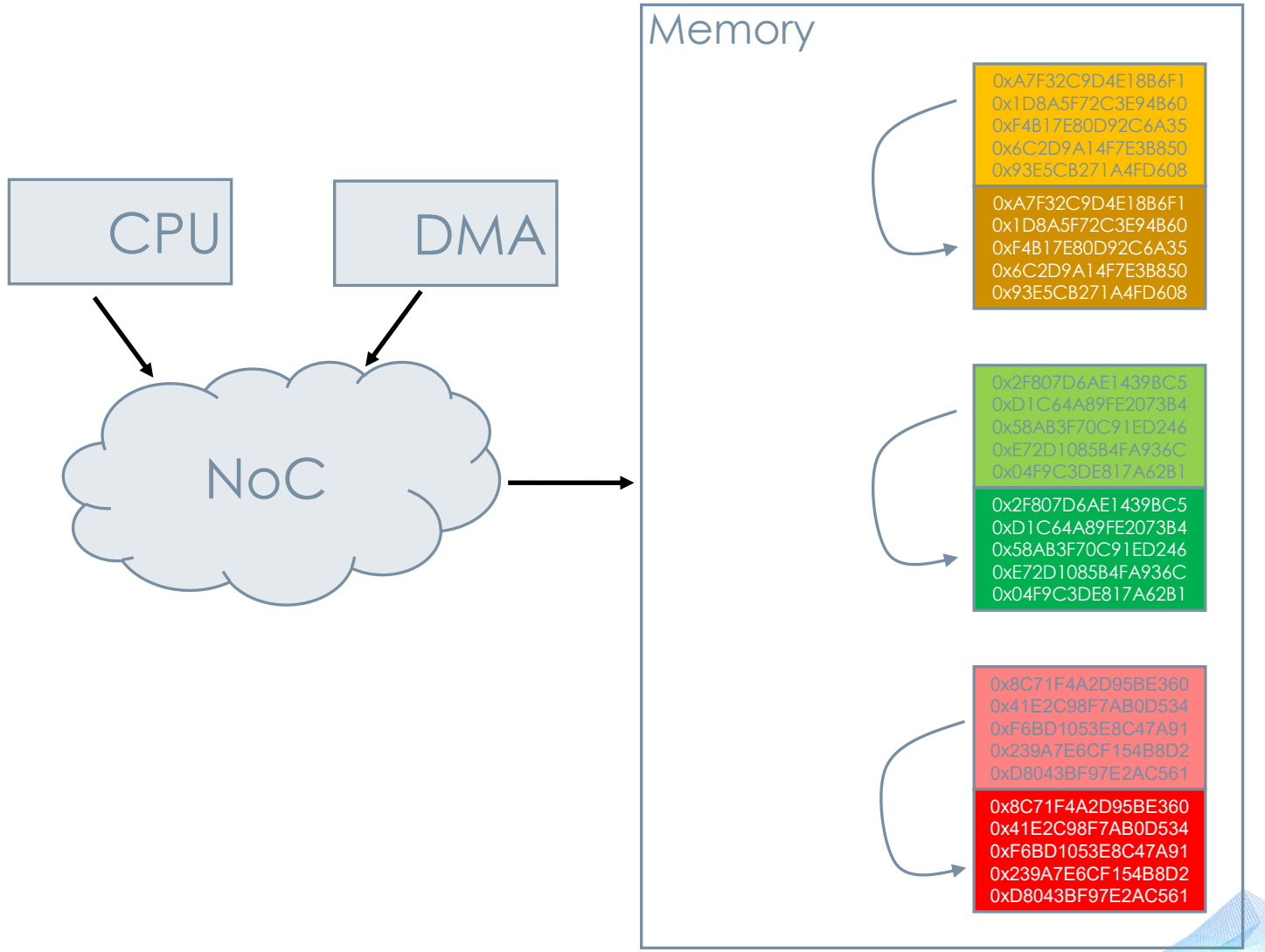
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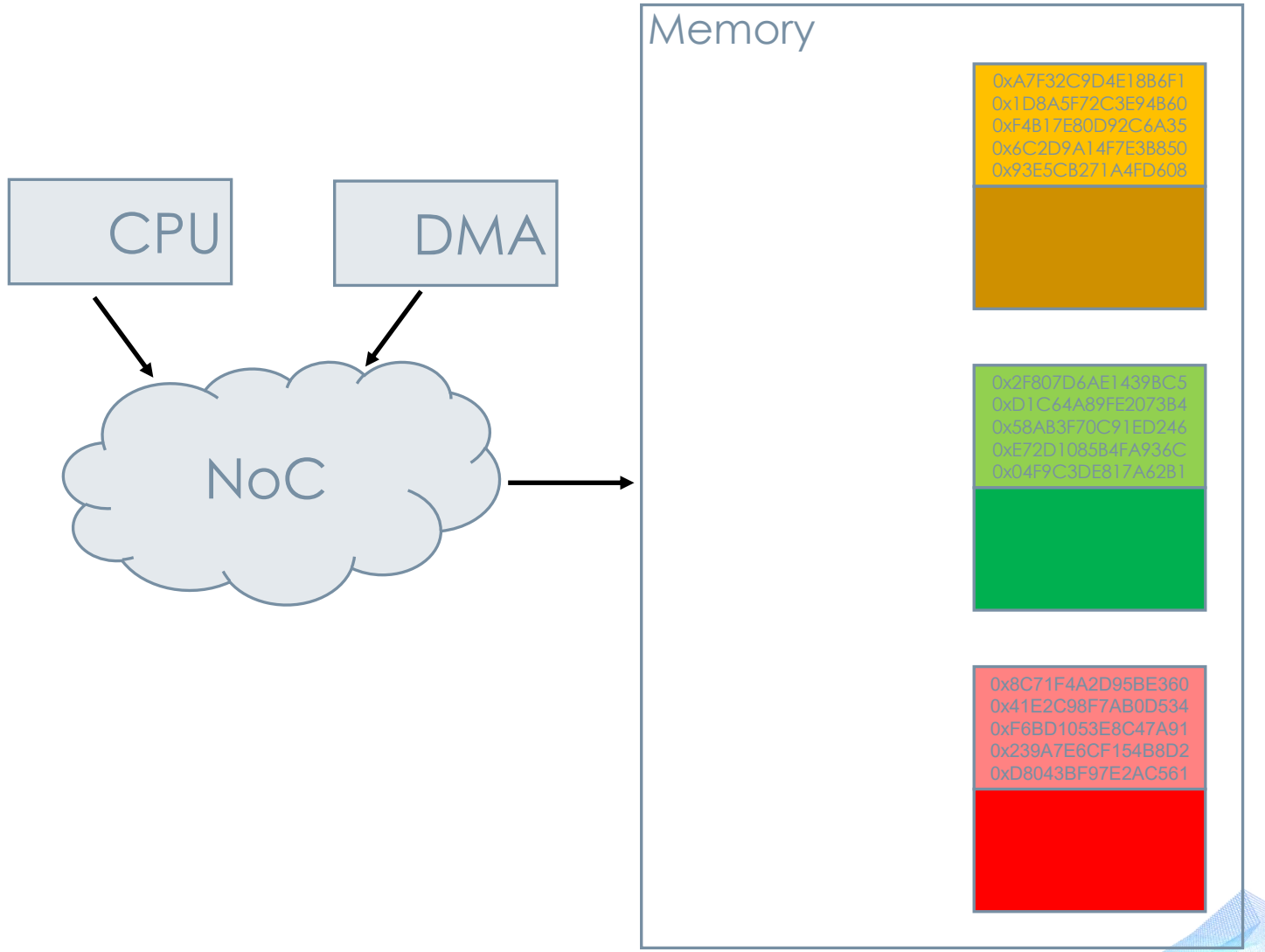
EXAMPLE: Descriptor based DMA walkthrough



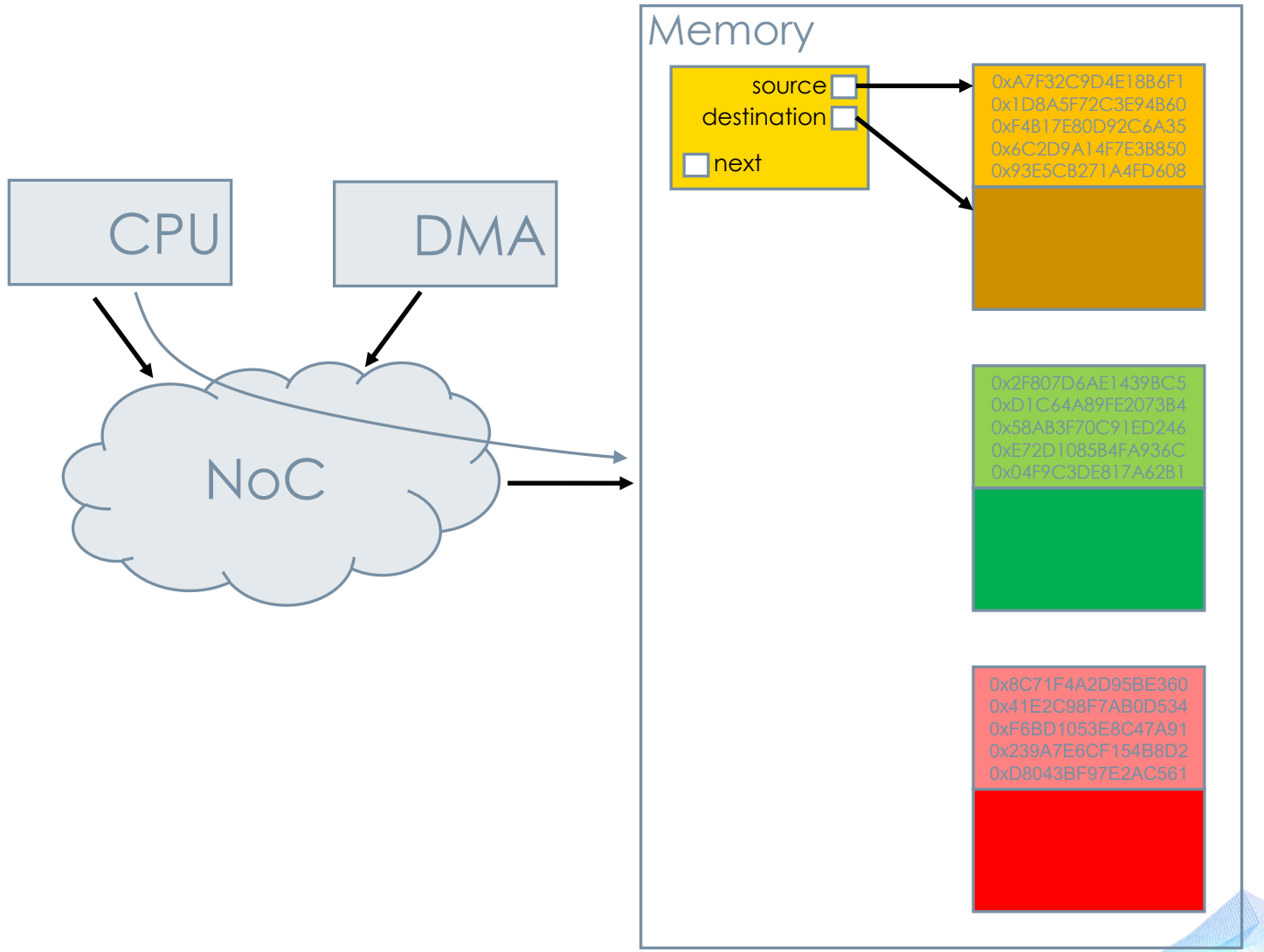
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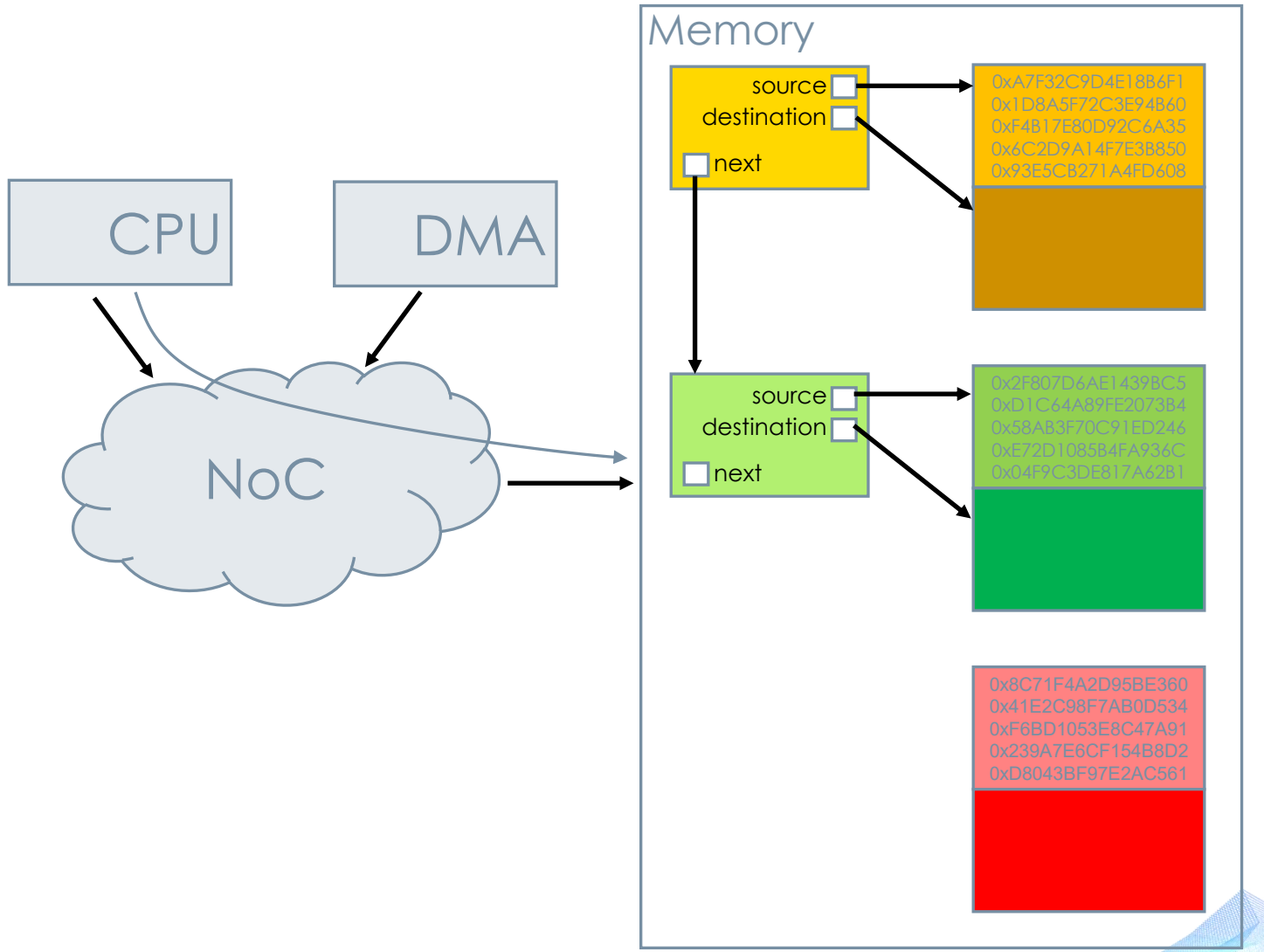
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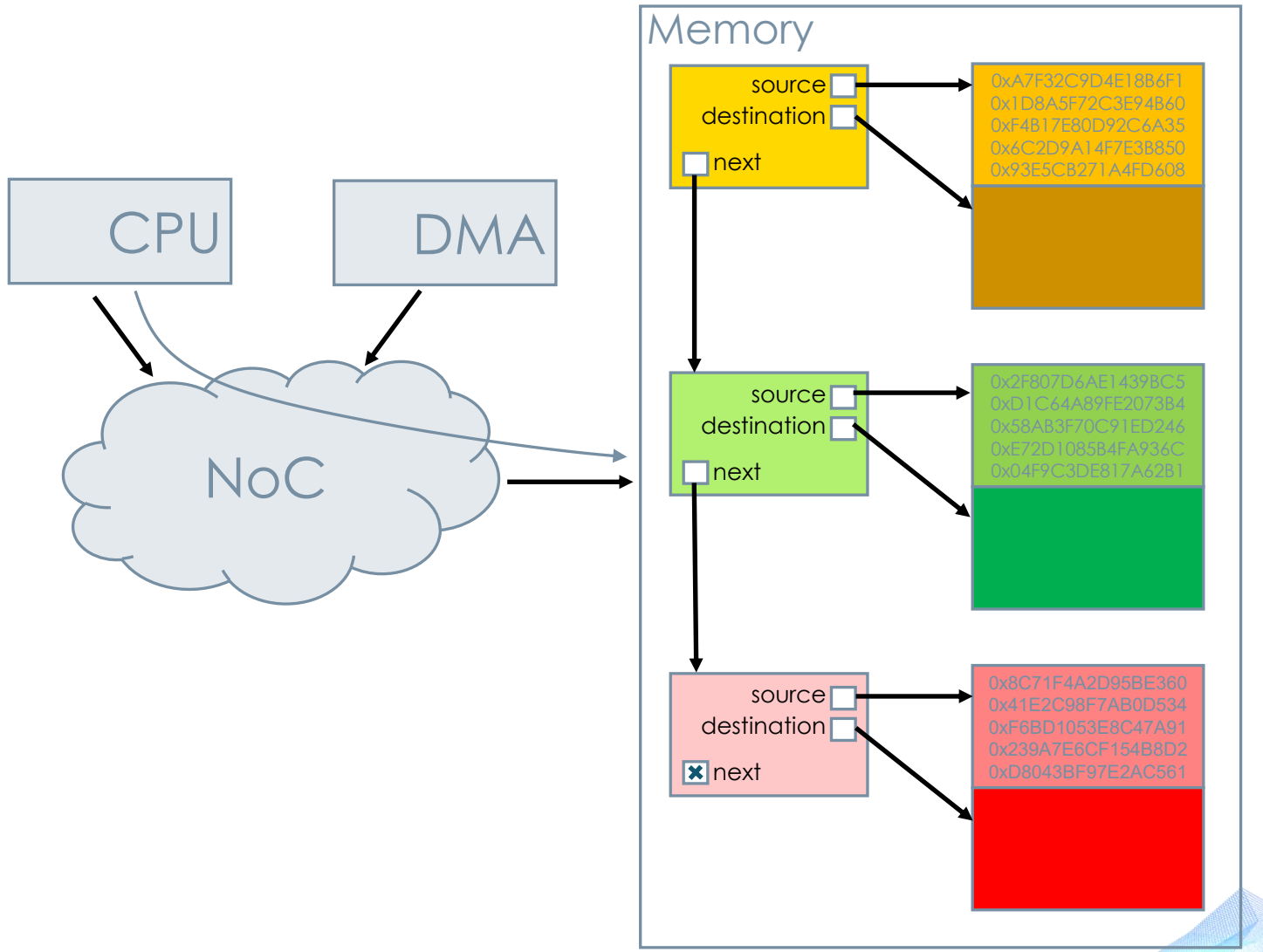
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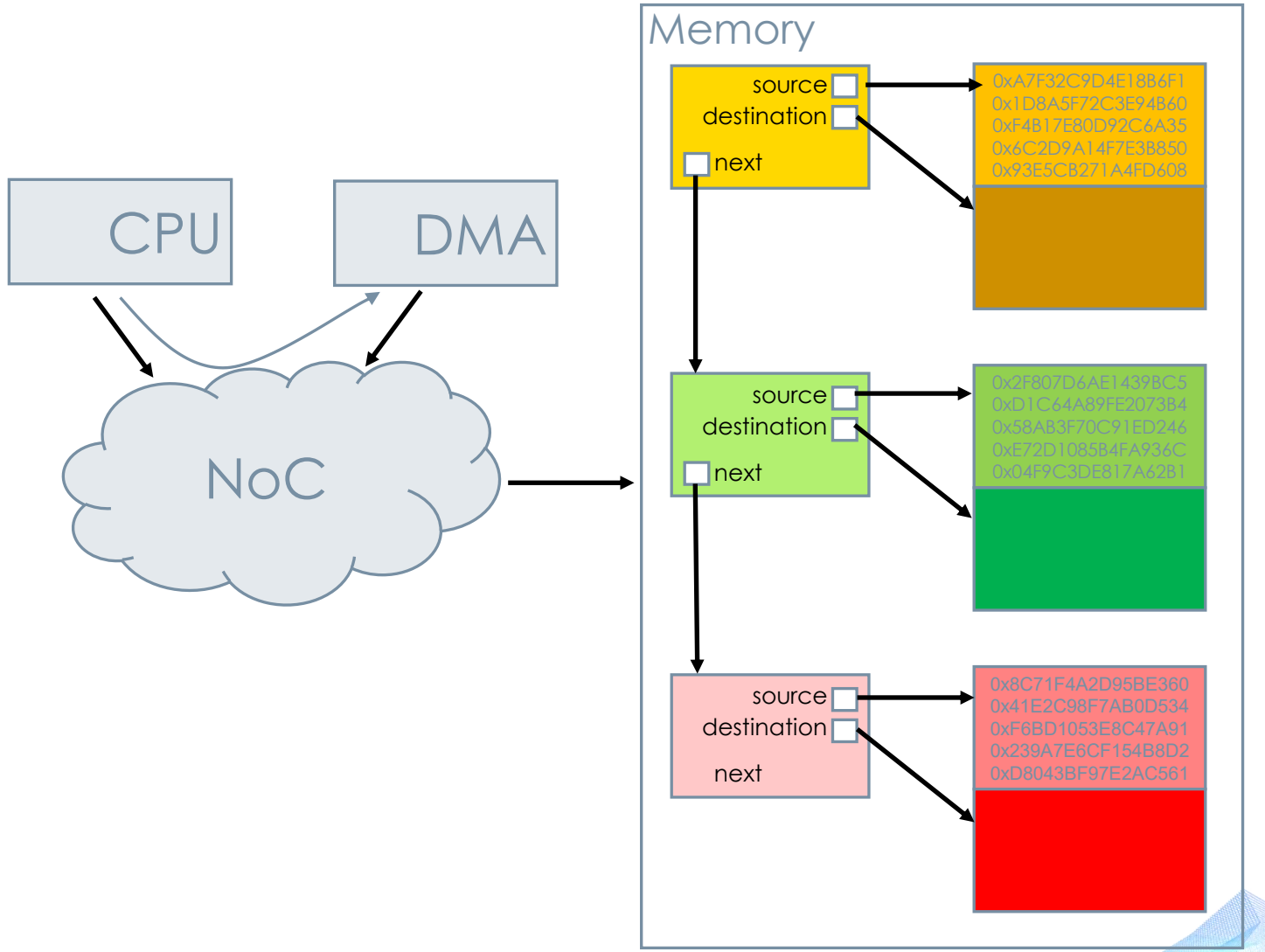
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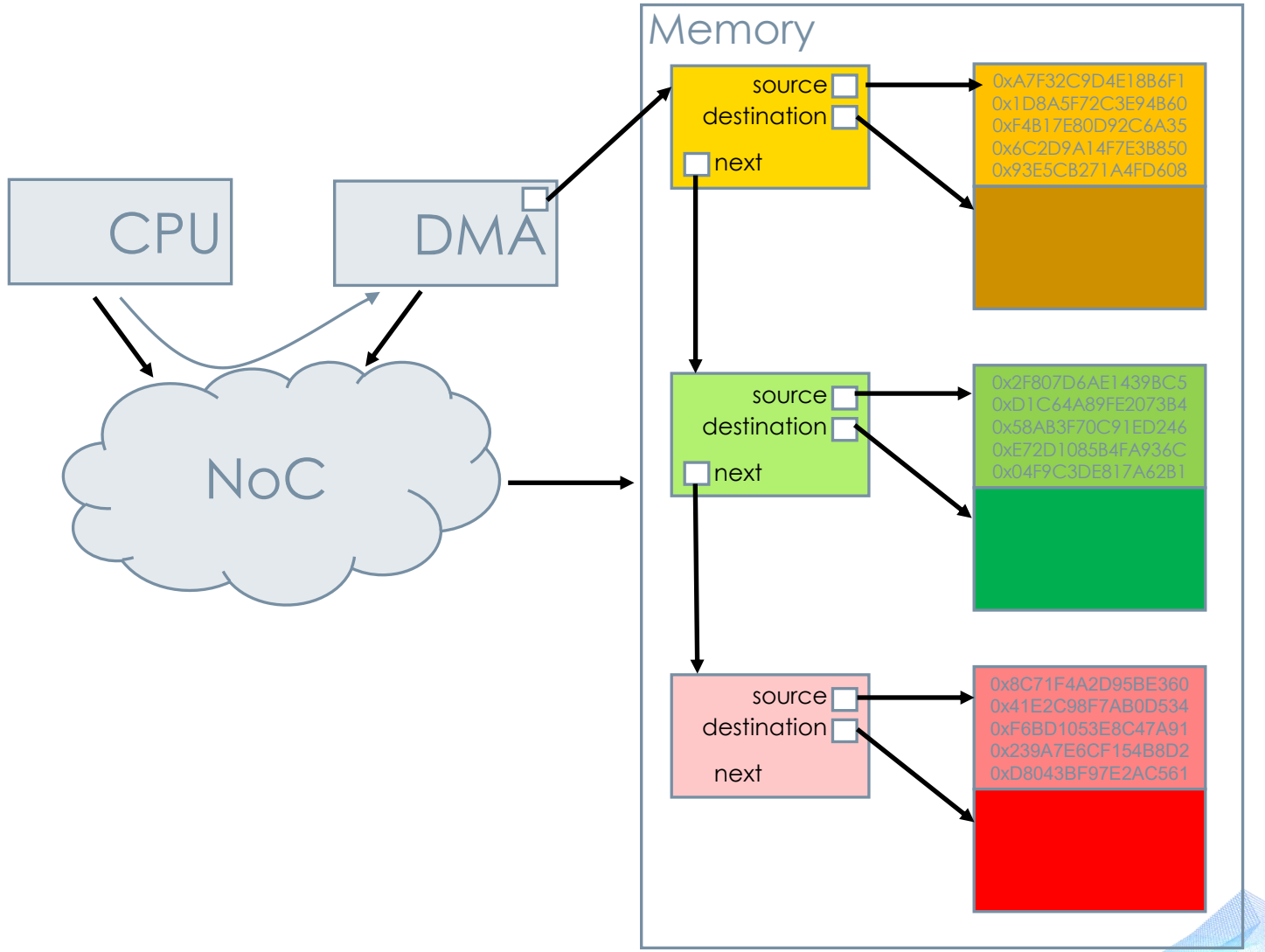
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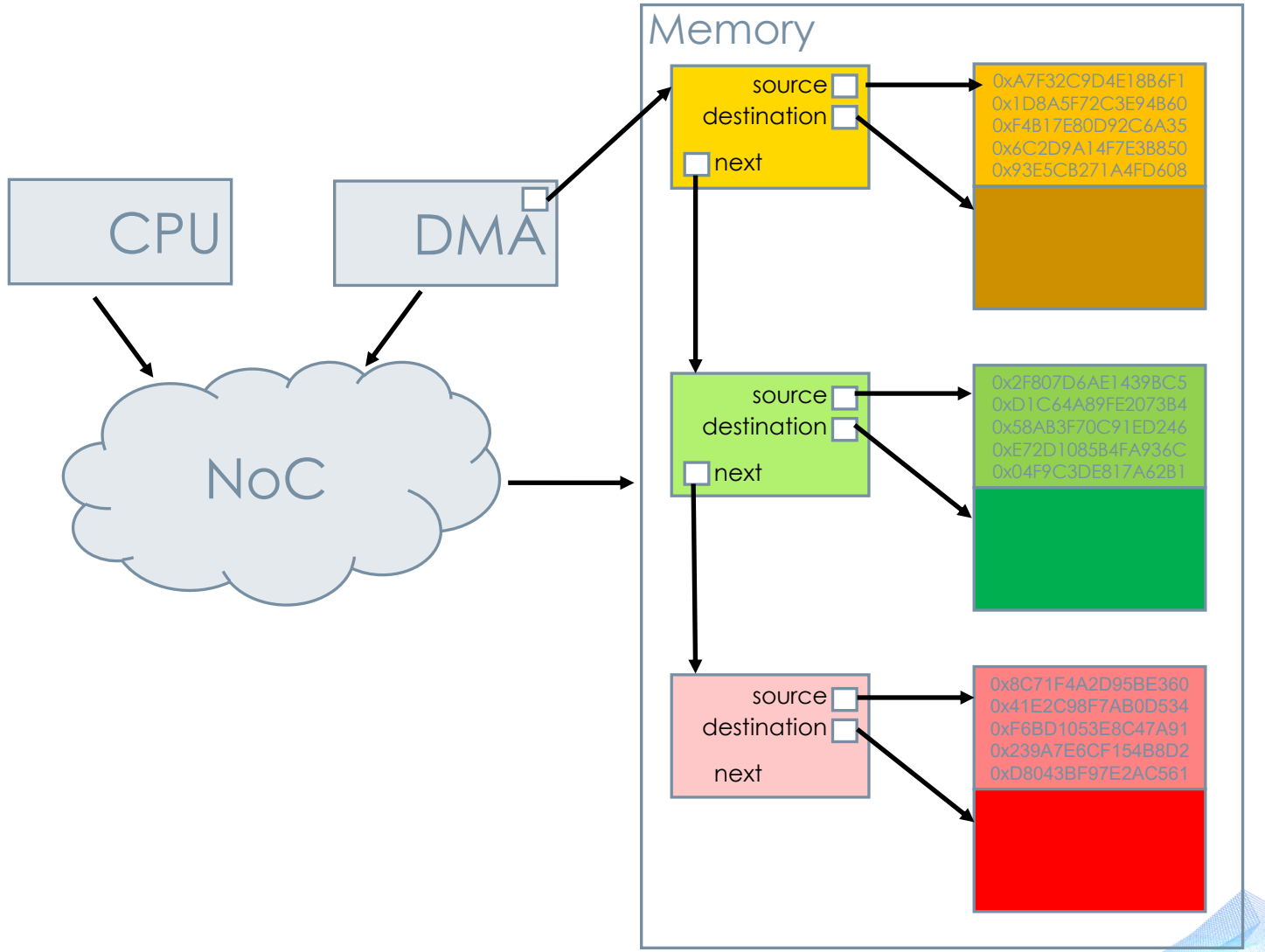
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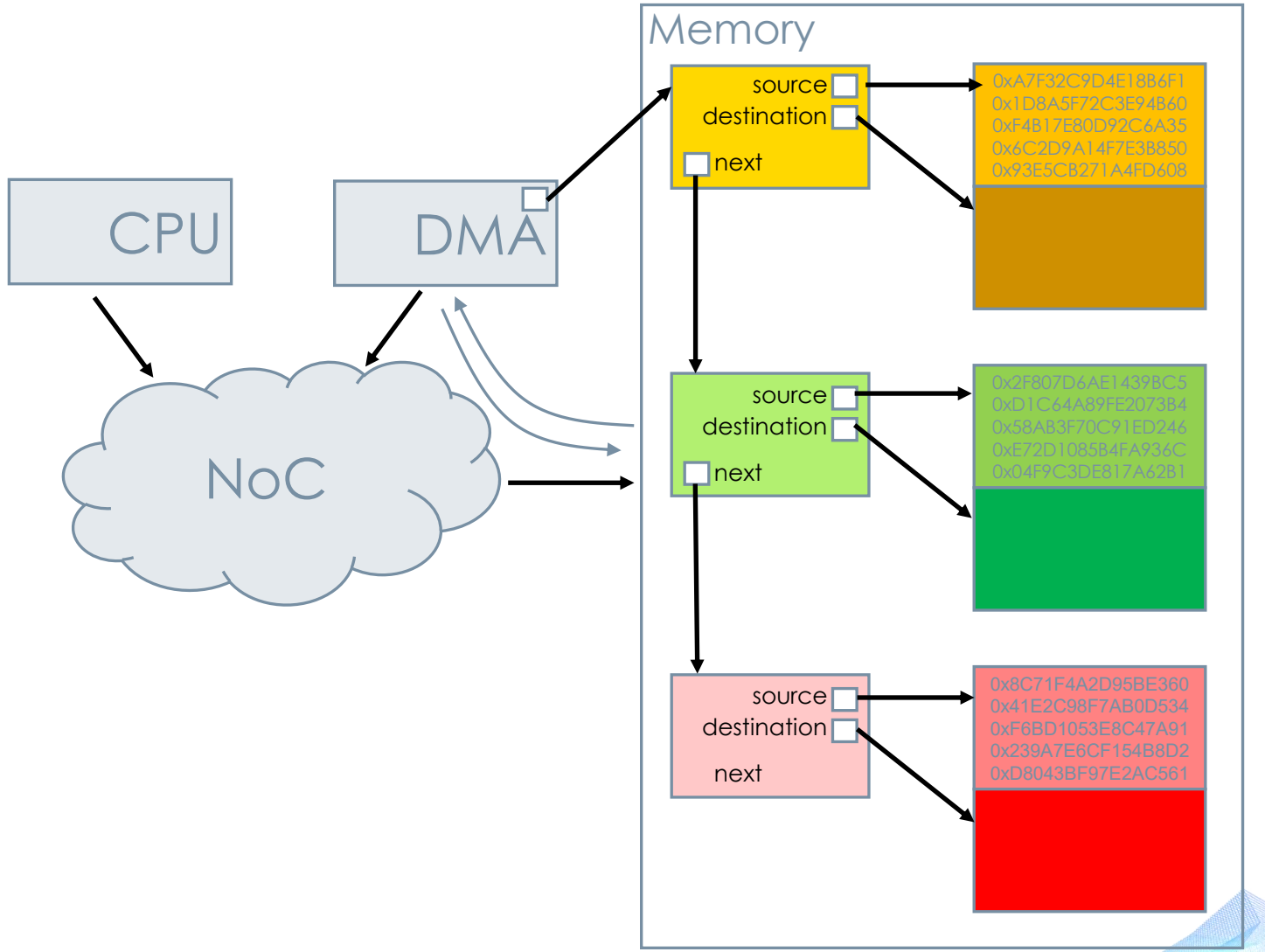
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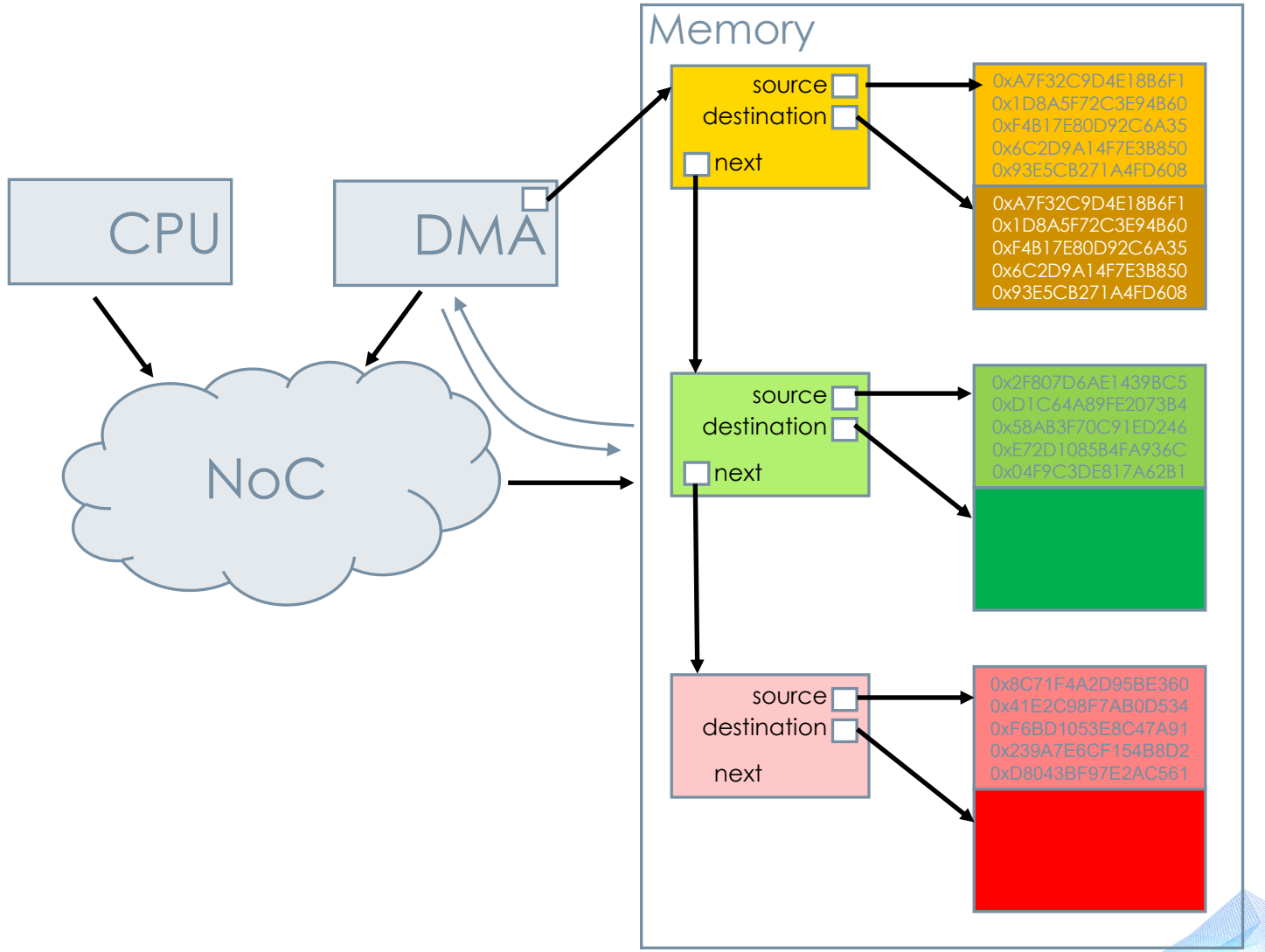
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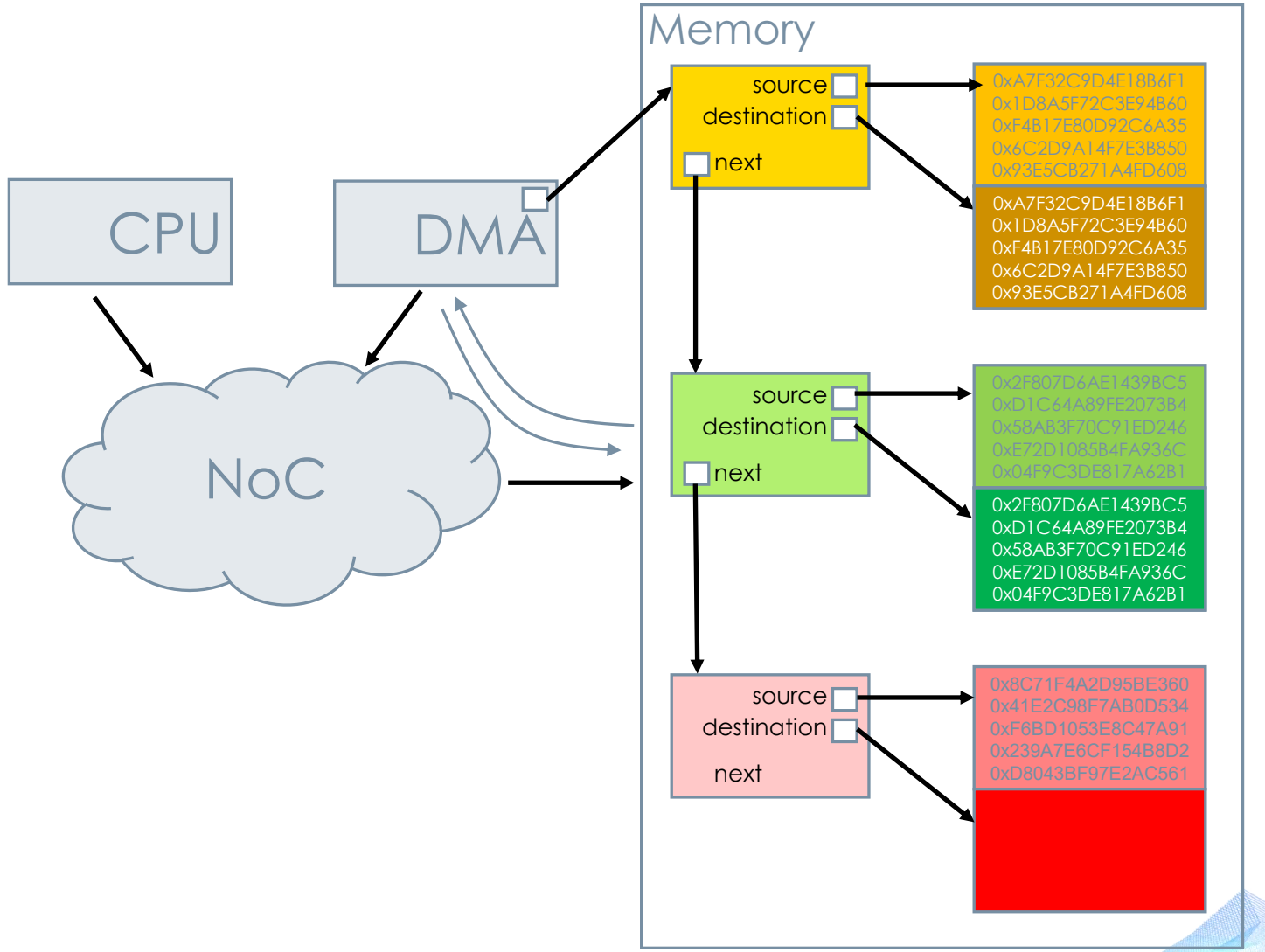
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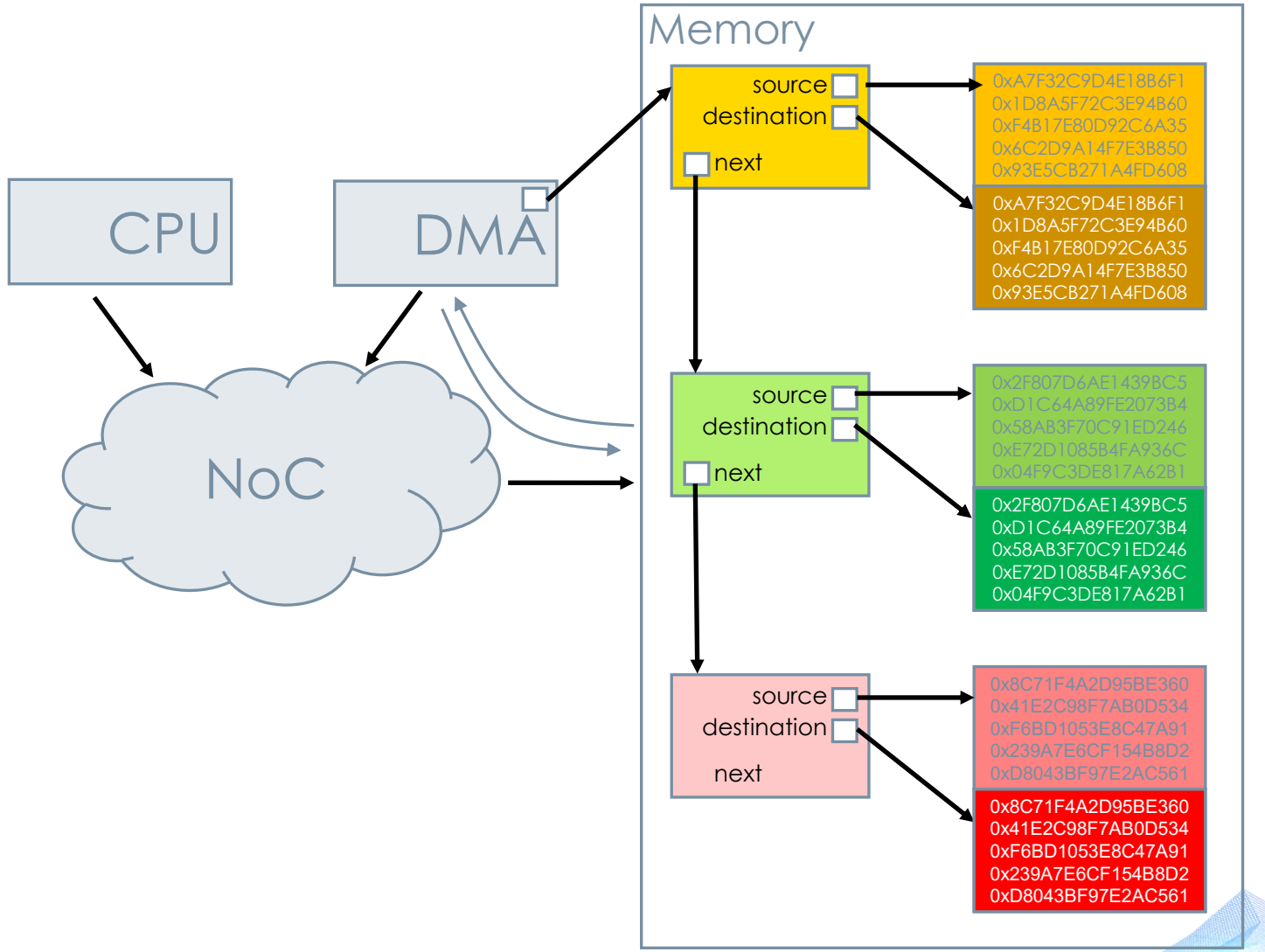
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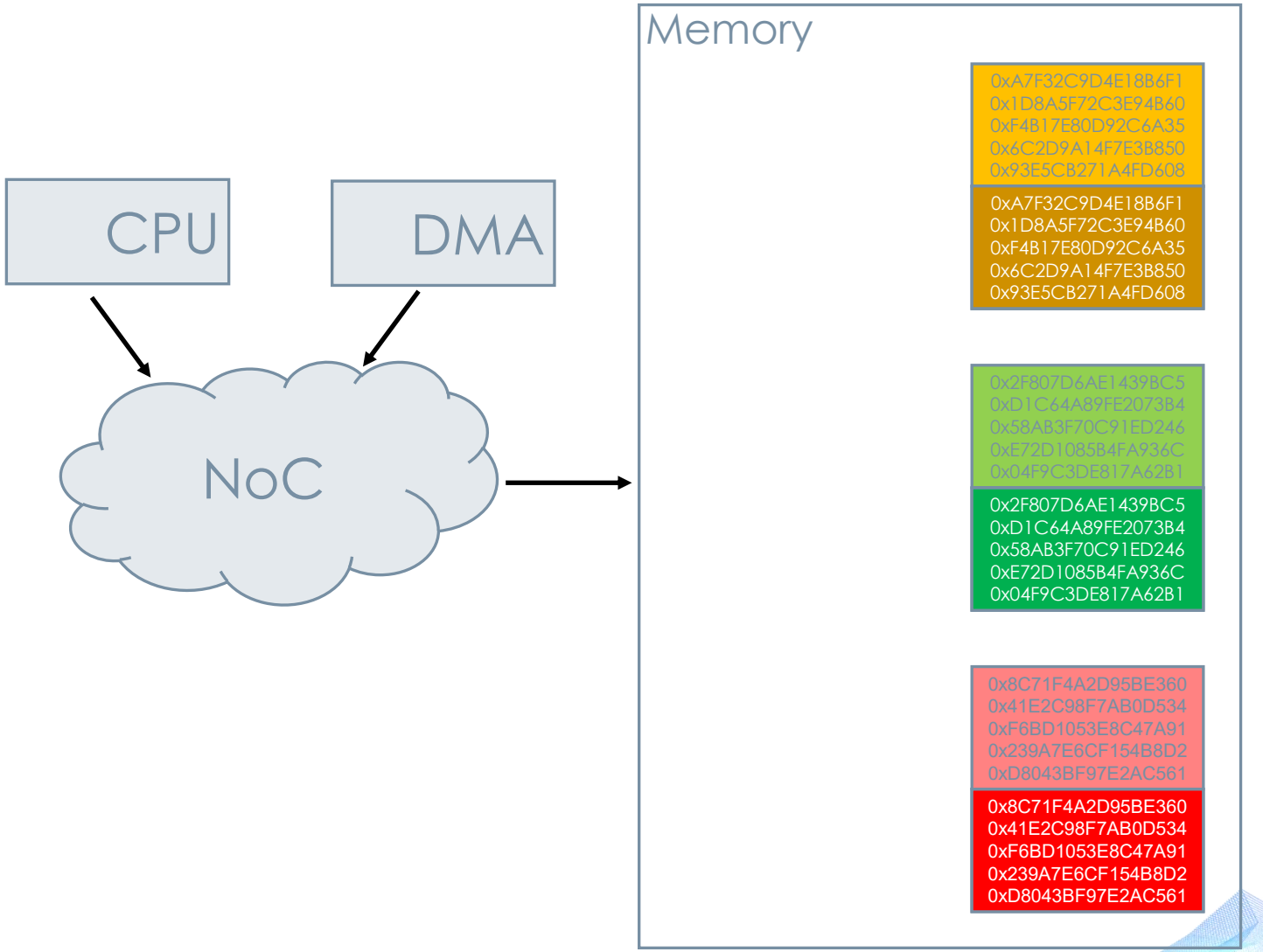
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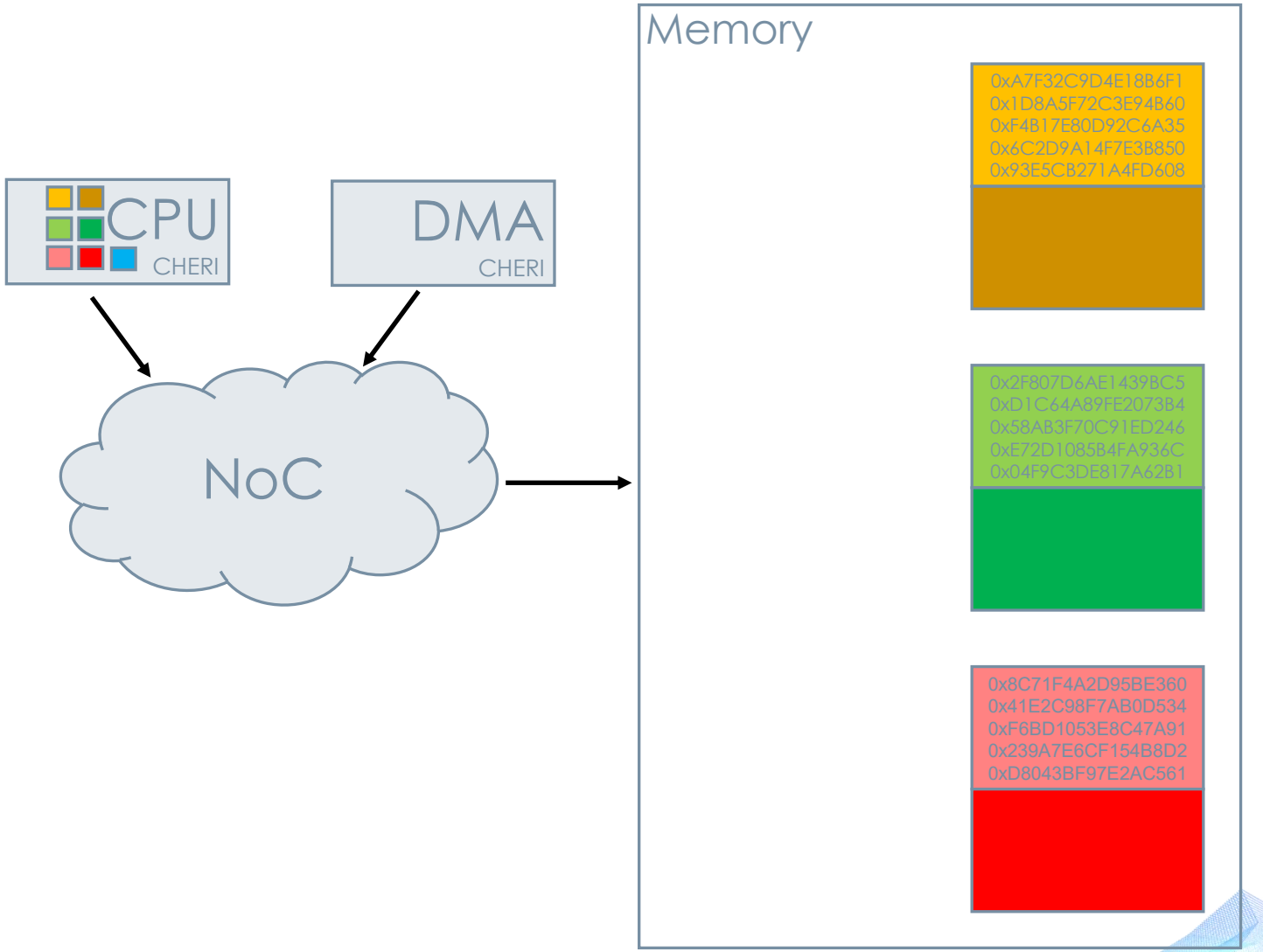
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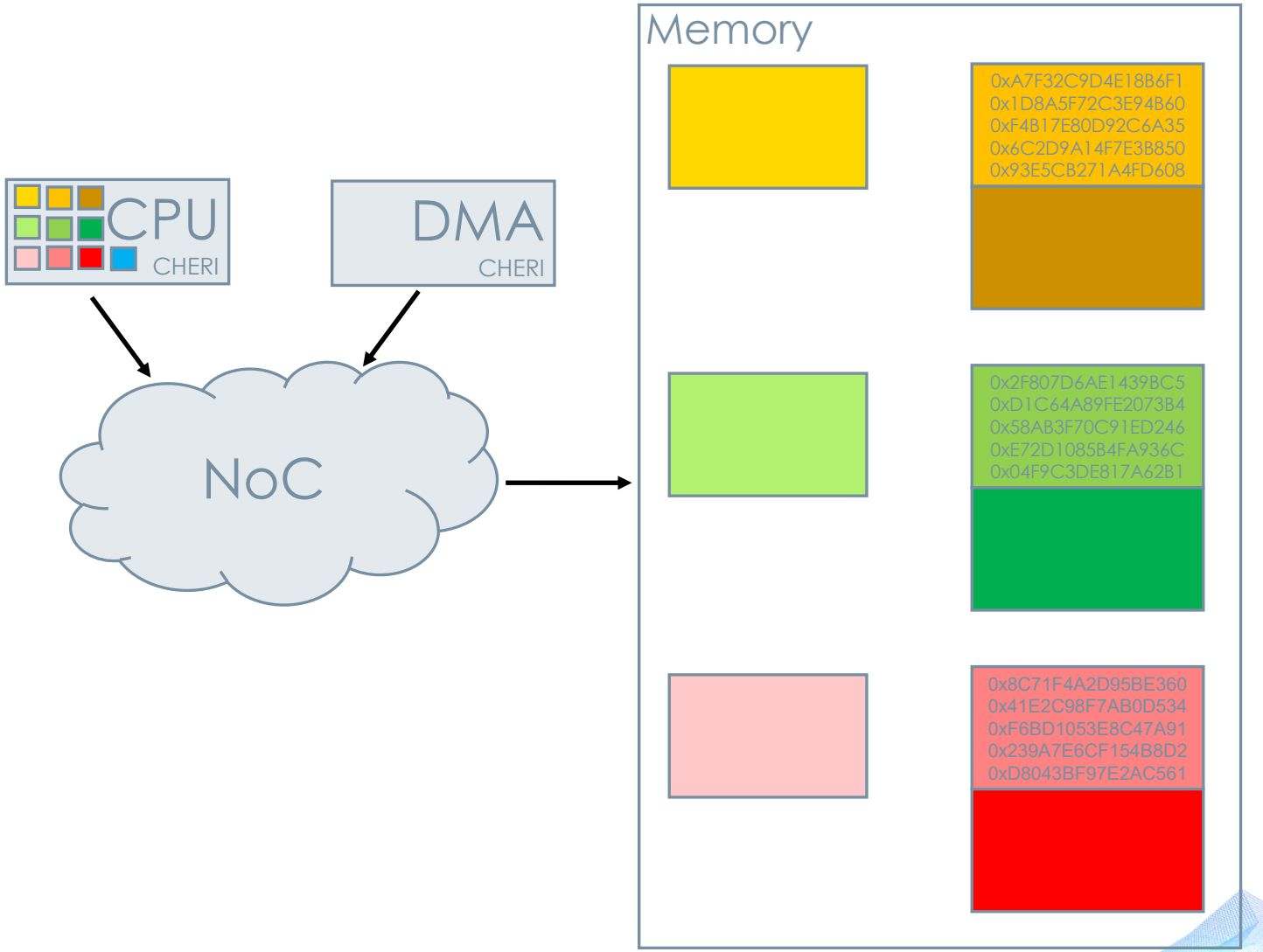
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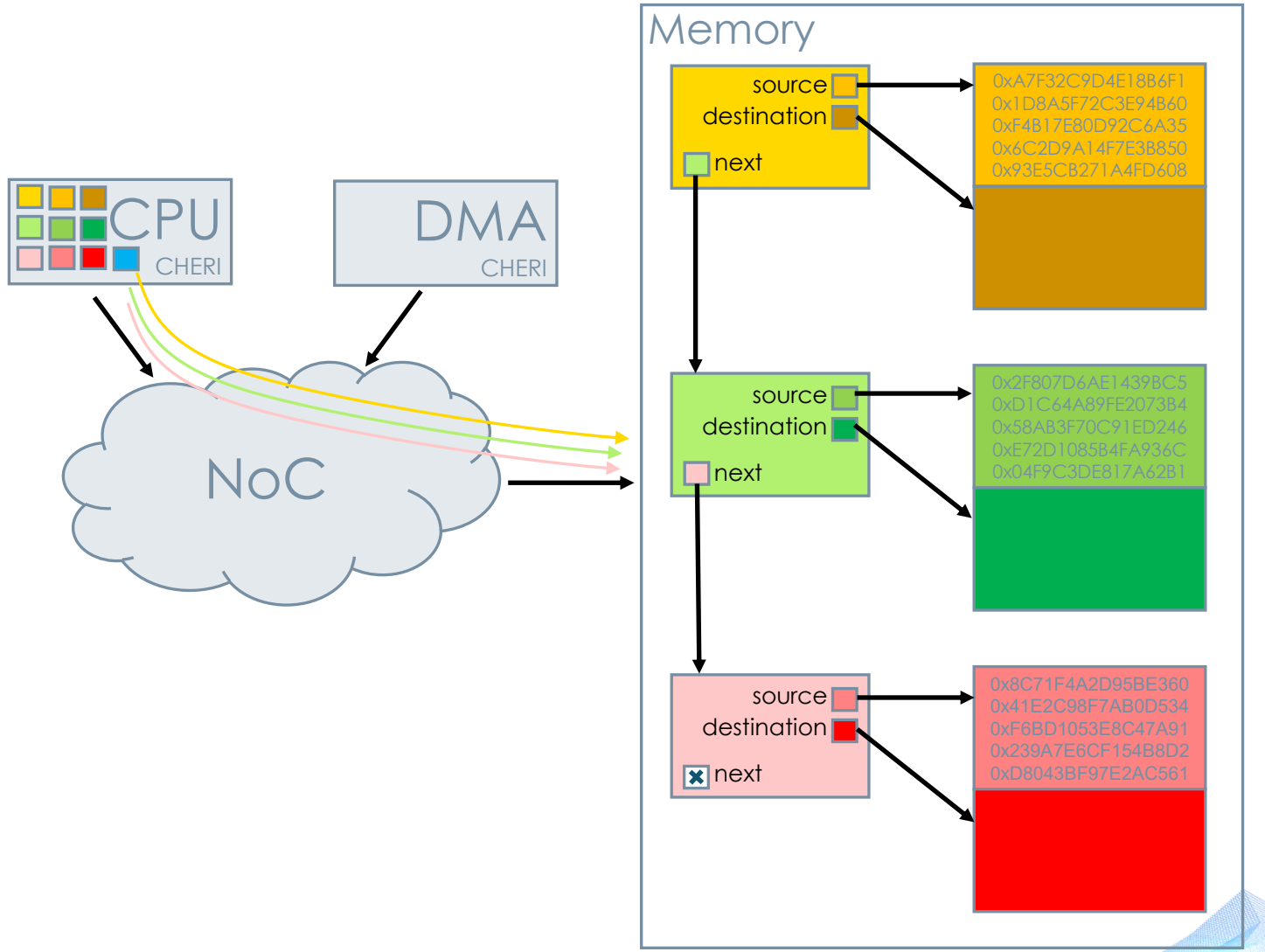
CHERI DMA


Memory
0xA7F32C9D4E18B6F1
0x1D8A5F72C3E94B60
0xF4B17E80D92C6A35
0x6C2D9A14F7E3B850
0x93E5CB271A4FD608
0x2F807D6AE1439BC5
0xD1C64A89FE2073B4
0x58AB3F70C91ED246
0xE72D1085B4FA936C
0x04F9C3DE817A62B1
0x8C71F4A2D95BE360
0x41E2C98F7AB0D534
0xF6BD1053E8C47A91
0x239A7E6CF154B8D2
0xD8043BF97E2AC561
CPU
CHERI
DMA
CHERI
NoC

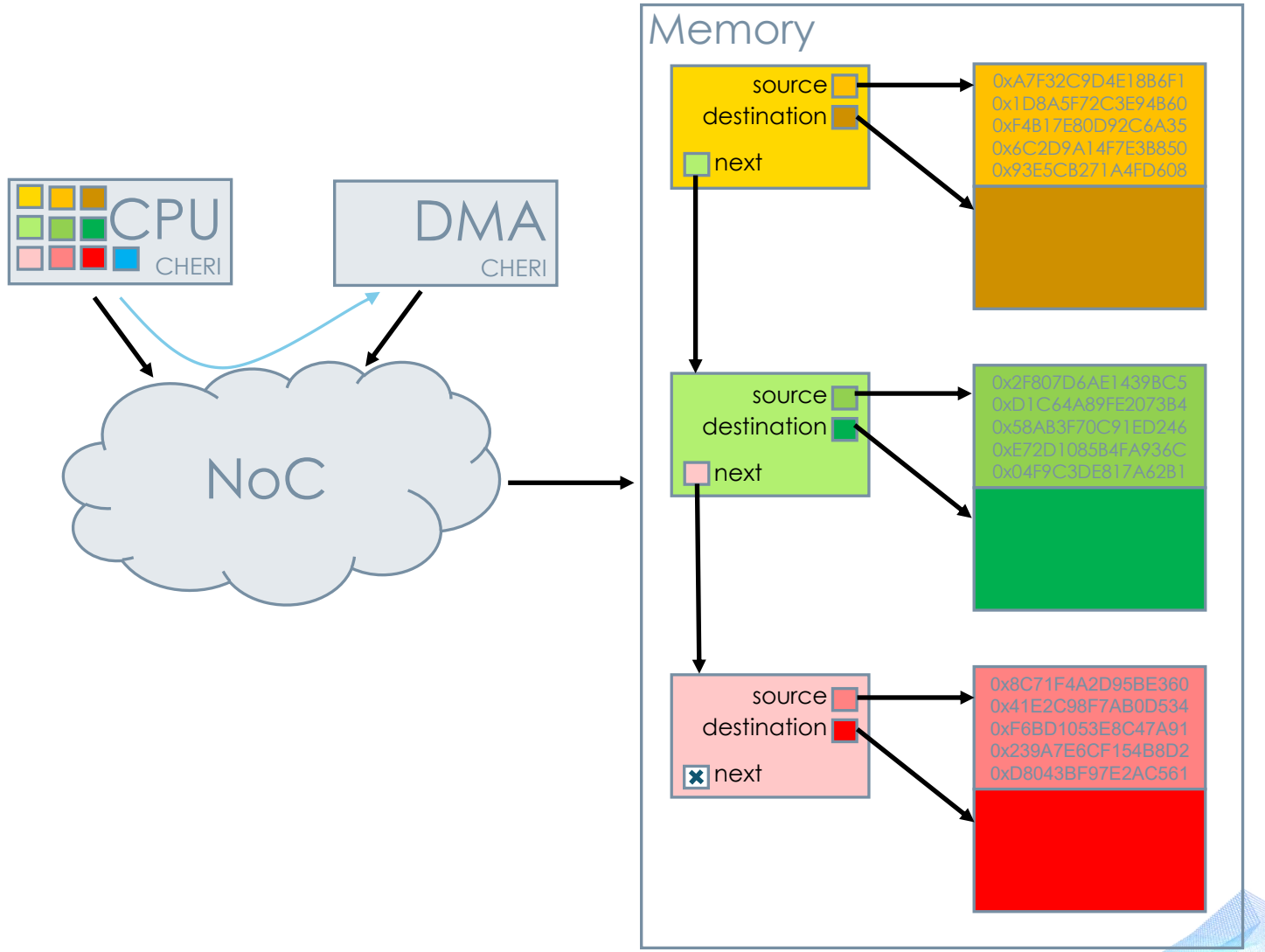
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CPU
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DMA
CHERI
NoC
Memory
0xA7F32C9D4E18B6F1
0x1D8A5F72C3E94B60
0xF4B17E80D92C6A35
0x6C2D9A14F7E3B850
0x93E5CB271A4FD608
0x2F807D6AE1439BC5
0xD1C64A89FE2073B4
0x58AB3F70C91ED246
0xE72D1085B4FA936C
0x04F9C3DE817A62B1
0x8C71F4A2D95BE360
0x41E2C98F7AB0D534
0xF6BD1053E8C47A91
0x239A7E6CF154B8D2
0xD8043BF97E2AC561

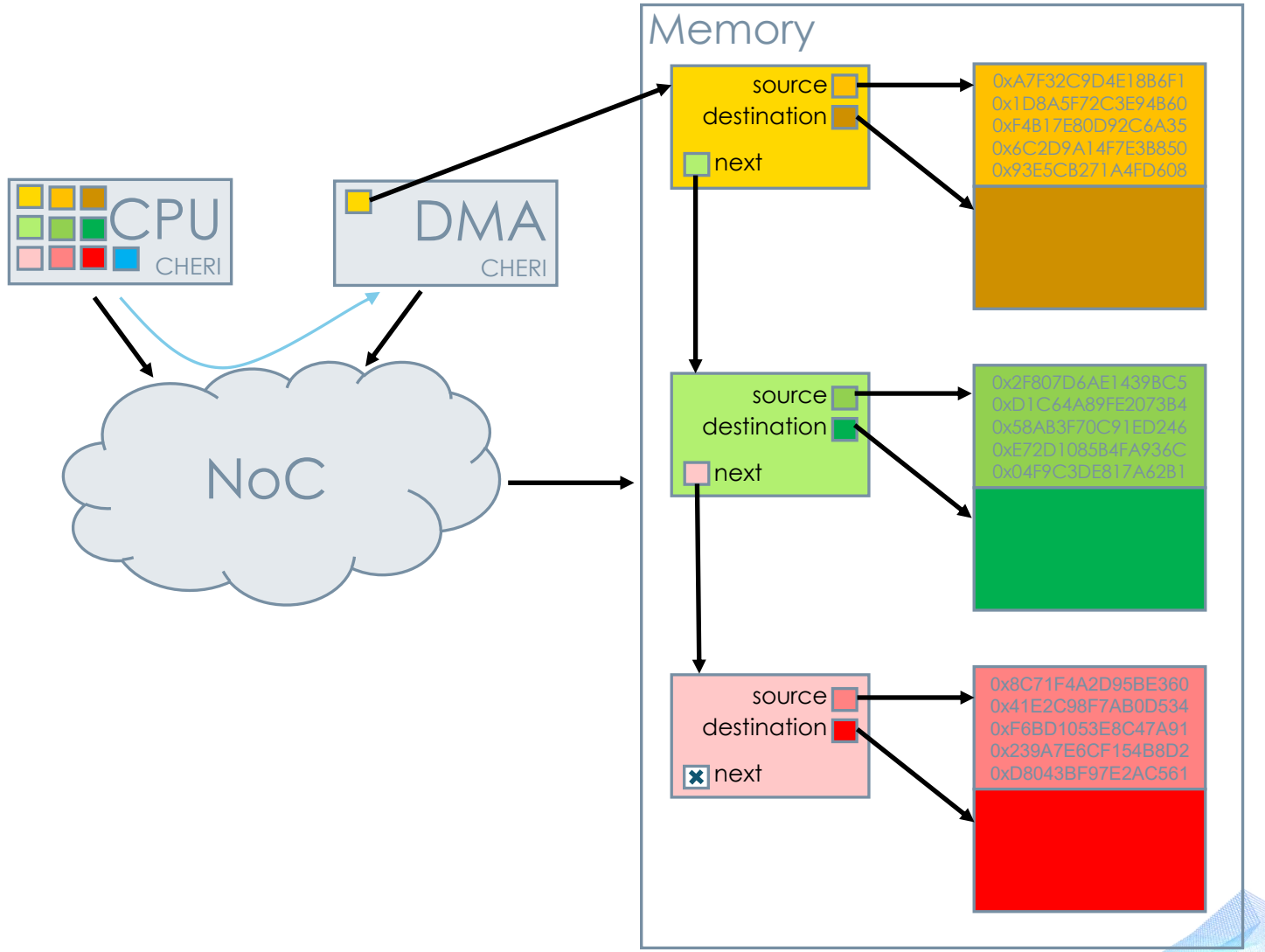
CHERI DMA


Memory
CPU
CHERI
DMA
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source
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next
0xA7F32C9D4E18B6F1
0x1D8A5F72C3E94B60
0xF4B17E80D92C6A35
0x6C2D9A14F7E3B850
0x93E5CB271A4FD608
source
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0x2F807D6AE1439BC5
0xD1C64A89FE2073B4
0x58AB3F70C91ED246
0xE72D1085B4FA936C
0x04F9C3DE817A62B1
source
destination
next
0x8C71F4A2D95BE360
0x41E2C98F7AB0D534
0xF6BD1053E8C47A91
0x239A7E6CF154B8D2
0xD8043BF97E2AC561

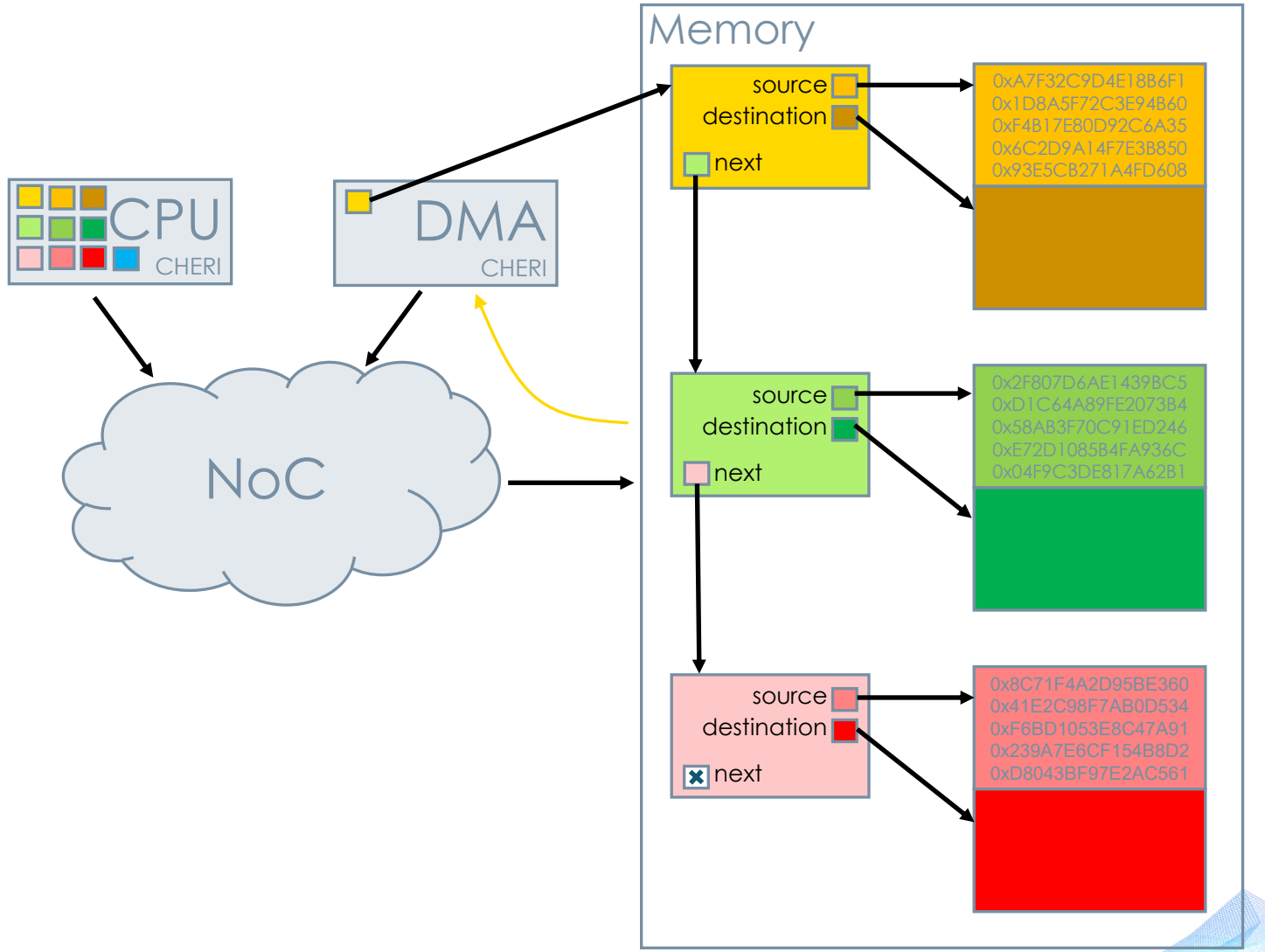
CHERI DMA


Memory
source
destination
next
0xA7F32C9D4E18B6F1
0x1D8A5F72C3E94B60
0xF4B17E80D92C6A35
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0x93E5CB271A4FD608
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0x2F807D6AE1439BC5
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0x58AB3F70C91ED246
0xE72D1085B4FA936C
0x04F9C3DE817A62B1
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0x8C71F4A2D95BE360
0x41E2C98F7AB0D534
0xF6BD1053E8C47A91
0x239A7E6CF154B8D2
0xD8043BF97E2AC561

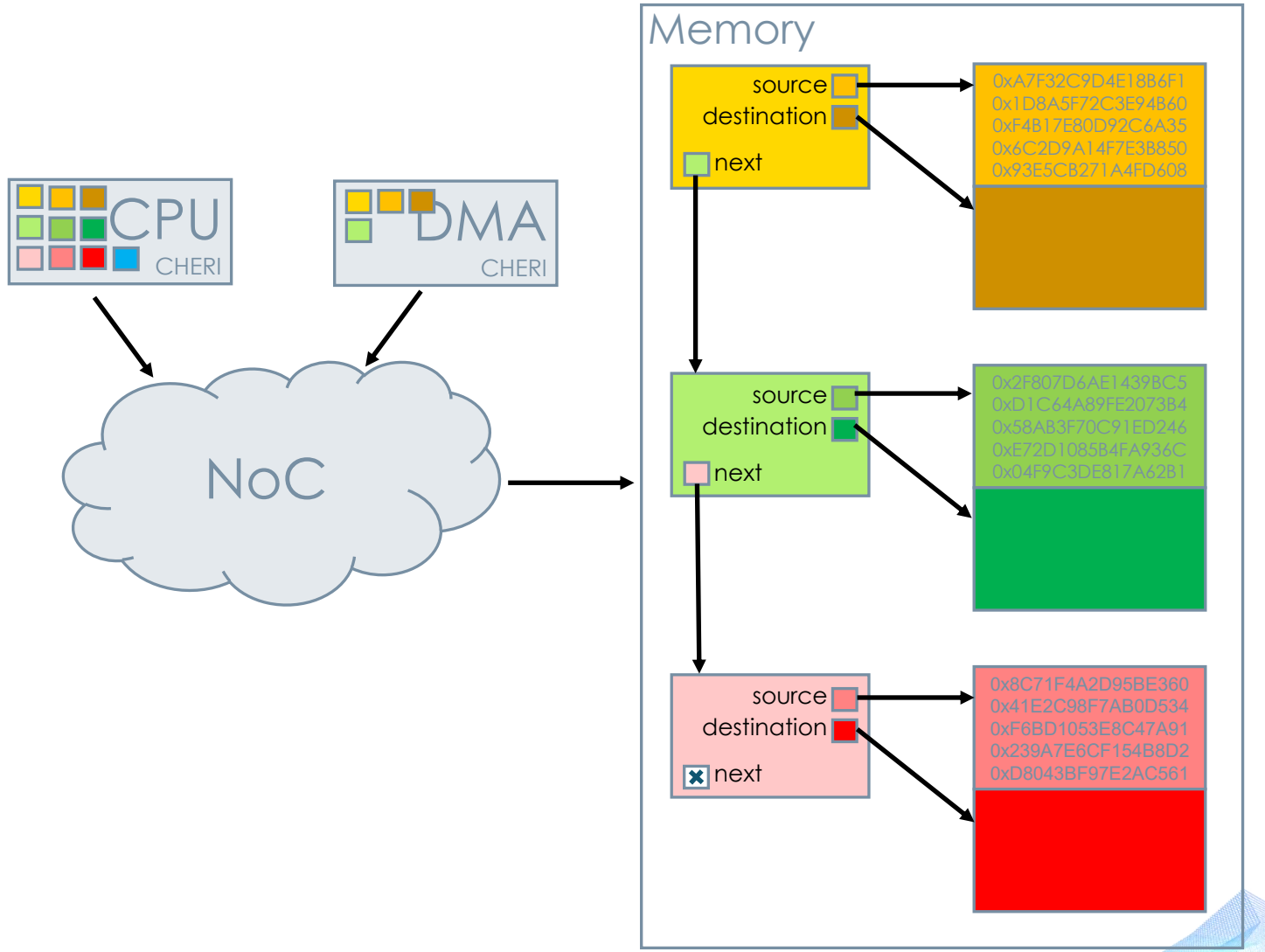
CHERI DMA


Memory
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next
0xA7F32C9D4E18B6F1
0x1D8A5F72C3E94B60
0xF4B17E80D92C6A35
0x6C2D9A14F7E3B850
0x93E5CB271A4FD608
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0x2F807D6AE1439BC5
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0x58AB3F70C91ED246
0xE72D1085B4FA936C
0x04F9C3DE817A62B1
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0x8C71F4A2D95BE360
0x41E2C98F7AB0D534
0xF6BD1053E8C47A91
0x239A7E6CF154B8D2
0xD8043BF97E2AC561

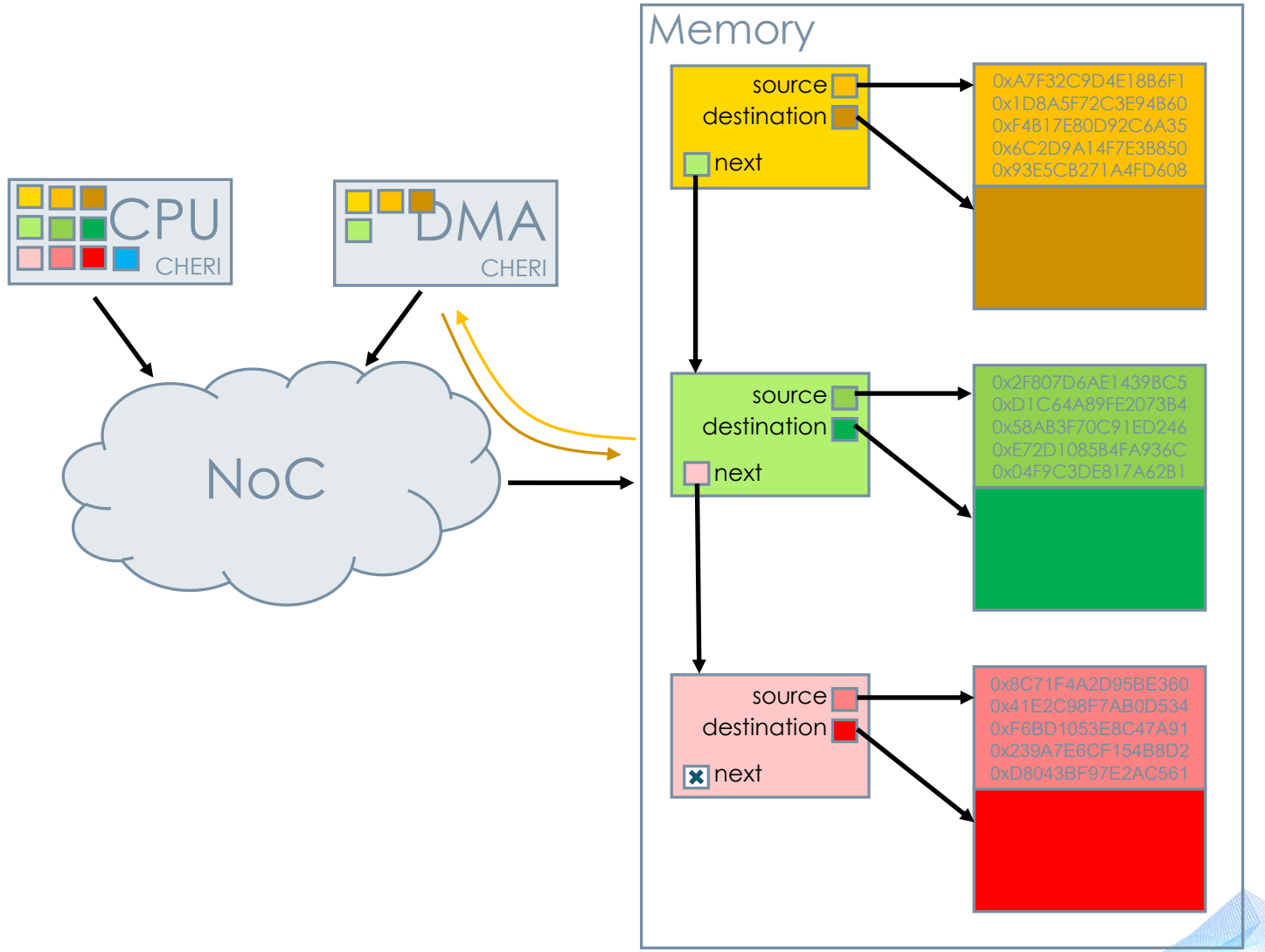
CHERI DMA


Memory
source
destination
next
0xA7F32C9D4E18B6F1
0x1D8A5F72C3E94B60
0xF4B17E80D92C6A35
0x6C2D9A14F7E3B850
0x93E5CB271A4FD608
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0x58AB3F70C91ED246
0xE72D1085B4FA936C
0x04F9C3DE817A62B1
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0x41E2C98F7AB0D534
0xF6BD1053E8C47A91
0x239A7E6CF154B8D2
0xD8043BF97E2AC561

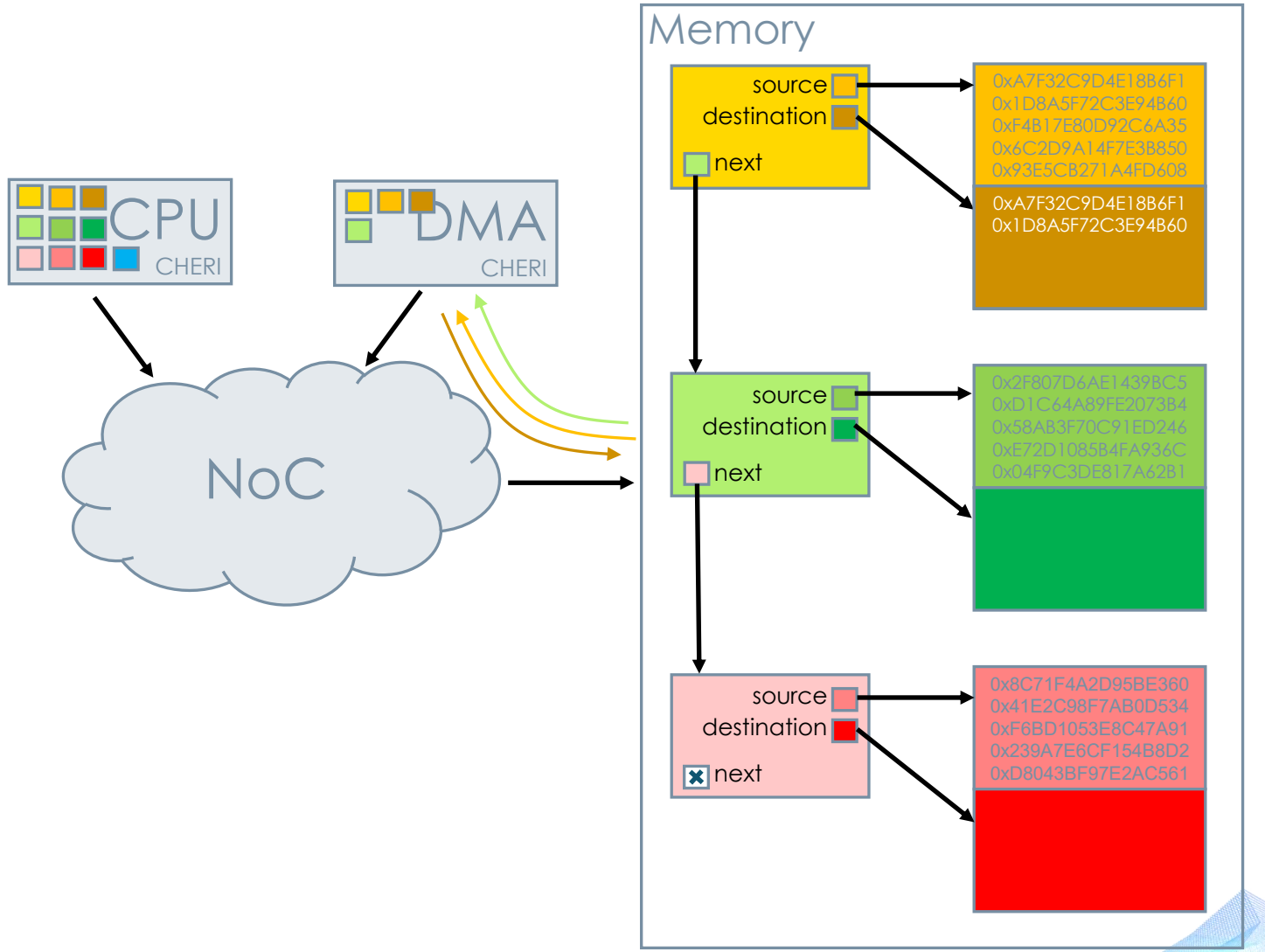
CHERI DMA


Memory
CPU
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source
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next
0xA7F32C9D4E18B6F1
0x1D8A5F72C3E94B60
0xF4B17E80D92C6A35
0x6C2D9A14F7E3B850
0x93E5CB271A4FD608
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0x2F807D6AE1439BC5
0xD1C64A89FE2073B4
0x58AB3F70C91ED246
0xE72D1085B4FA936C
0x04F9C3DE817A62B1
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0x8C71F4A2D95BE360
0x41E2C98F7AB0D534
0xF6BD1053E8C47A91
0x239A7E6CF154B8D2
0xD8043BF97E2AC561

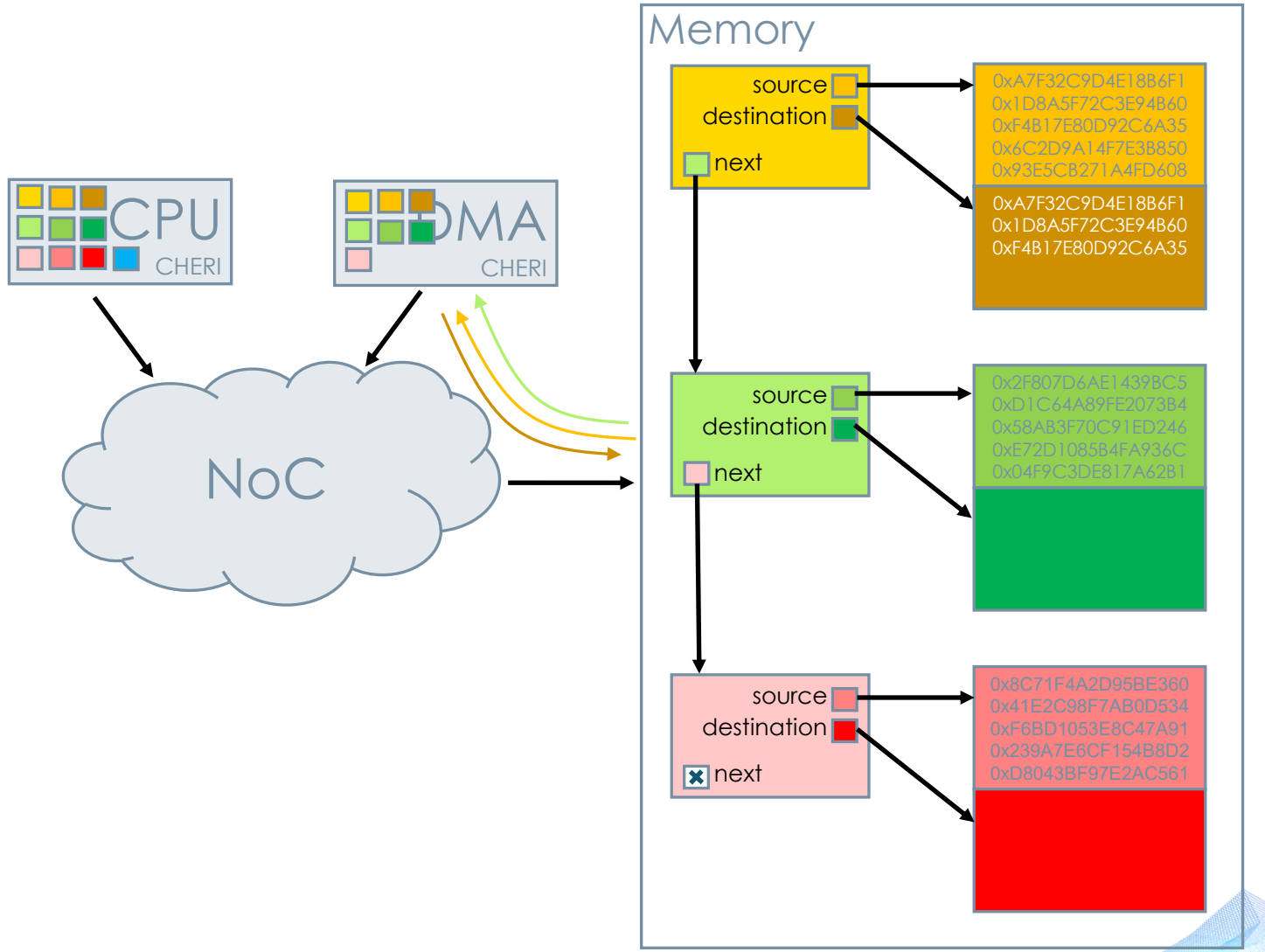
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0xA7F32C9D4E18B6F1
0x1D8A5F72C3E94B60
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0x93E5CB271A4FD608
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0x2F807D6AE1439BC5
0xD1C64A89FE2073B4
0x58AB3F70C91ED246
0xE72D1085B4FA936C
0x04F9C3DE817A62B1
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0x8C71F4A2D95BE360
0x41E2C98F7AB0D534
0xF6BD1053E8C47A91
0x239A7E6CF154B8D2
0xD8043BF97E2AC561

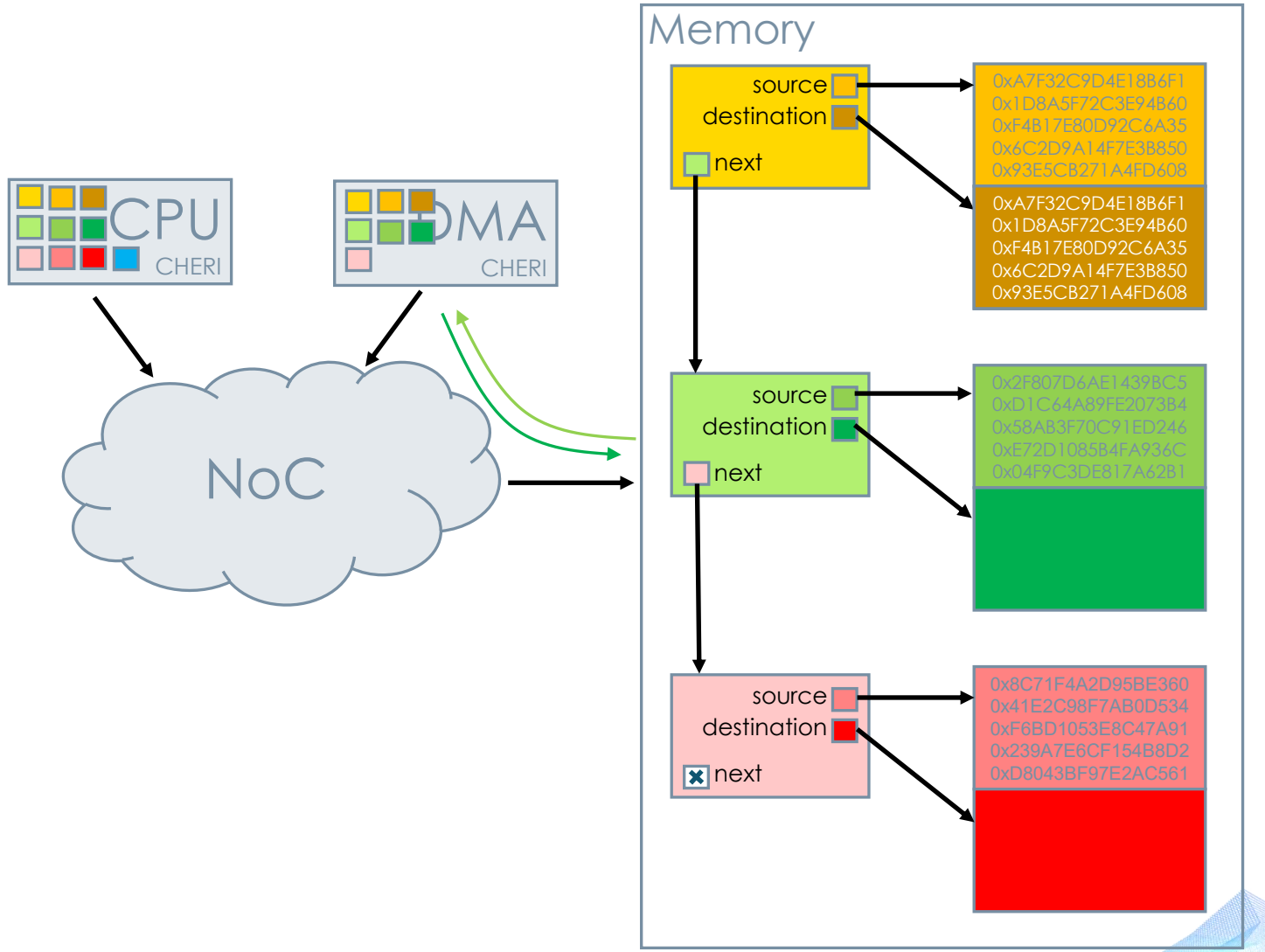
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Memory
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source
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next
0xA7F32C9D4E18B6F1
0x1D8A5F72C3E94B60
0xF4B17E80D92C6A35
0x6C2D9A14F7E3B850
0x93E5CB271A4FD608
0xA7F32C9D4E18B6F1
0x1D8A5F72C3E94B60
source
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0x2F807D6AE1439BC5
0xD1C64A89FE2073B4
0x58AB3F70C91ED246
0xE72D1085B4FA936C
0x04F9C3DE817A62B1
source
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0x8C71F4A2D95BE360
0x41E2C98F7AB0D534
0xF6BD1053E8C47A91
0x239A7E6CF154B8D2
0xD8043BF97E2AC561

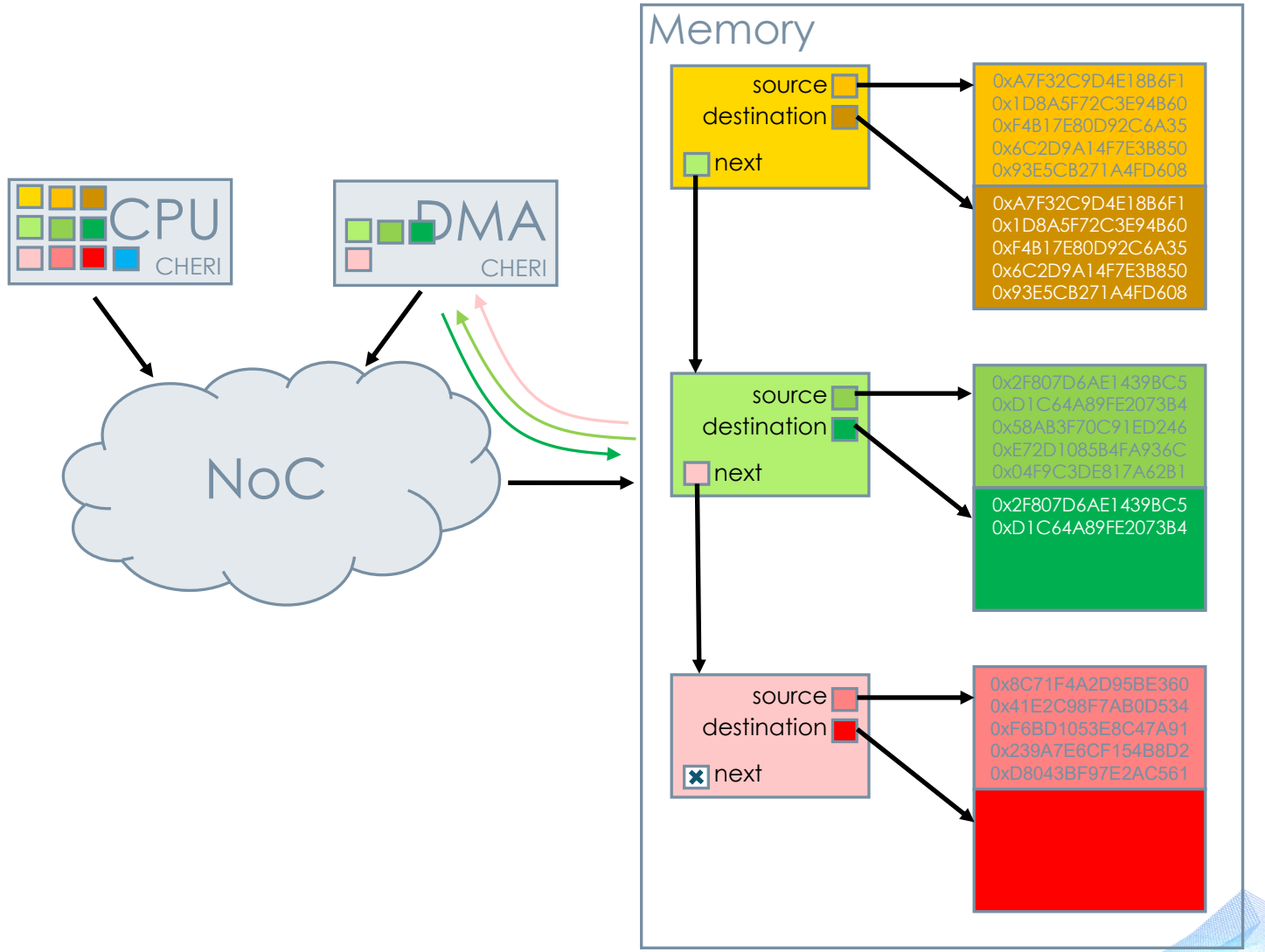
CHERI DMA


Memory
CPU
CHERI
DMA
CHERI
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source
destination
next
0xA7F32C9D4E18B6F1
0x1D8A5F72C3E94B60
0xF4B17E80D92C6A35
0x6C2D9A14F7E3B850
0x93E5CB271A4FD608
0xA7F32C9D4E18B6F1
0x1D8A5F72C3E94B60
0xF4B17E80D92C6A35
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0x2F807D6AE1439BC5
0xD1C64A89FE2073B4
0x58AB3F70C91ED246
0xE72D1085B4FA936C
0x04F9C3DE817A62B1
source
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next
0x8C71F4A2D95BE360
0x41E2C98F7AB0D534
0xF6BD1053E8C47A91
0x239A7E6CF154B8D2
0xD8043BF97E2AC561

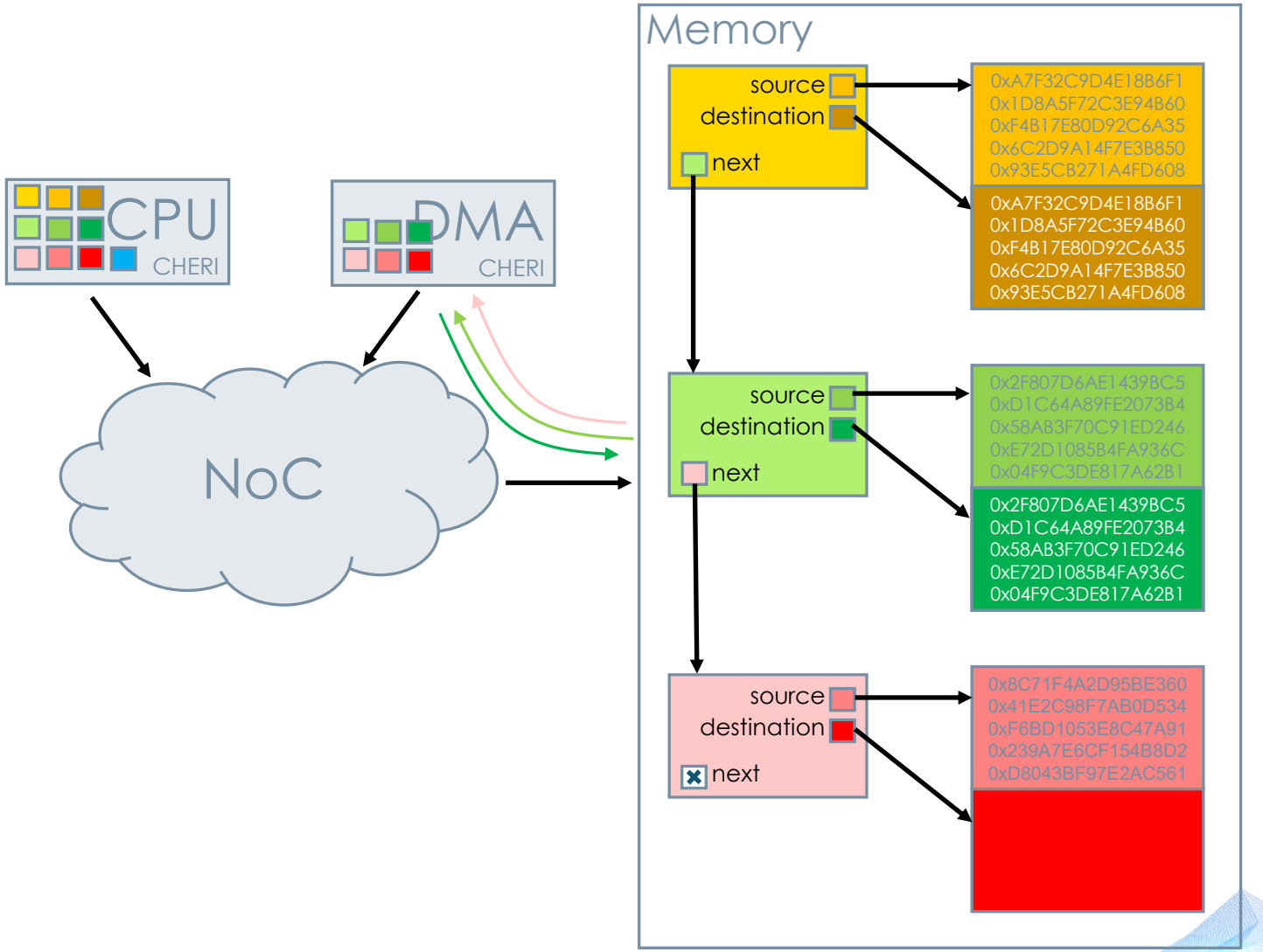
CHERI DMA


Memory
CPU
CHERI
DMA
CHERI
NoC
source
destination
next
0xA7F32C9D4E18B6F1
0x1D8A5F72C3E94B60
0xF4B17E80D92C6A35
0x6C2D9A14F7E3B850
0x93E5CB271A4FD608
0xA7F32C9D4E18B6F1
0x1D8A5F72C3E94B60
0xF4B17E80D92C6A35
0x6C2D9A14F7E3B850
0x93E5CB271A4FD608
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0x2F807D6AE1439BC5
0xD1C64A89FE2073B4
0x58AB3F70C91ED246
0xE72D1085B4FA936C
0x04F9C3DE817A62B1
source
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0x8C71F4A2D95BE360
0x41E2C98F7AB0D534
0xF6BD1053E8C47A91
0x239A7E6CF154B8D2
0xD8043BF97E2AC561

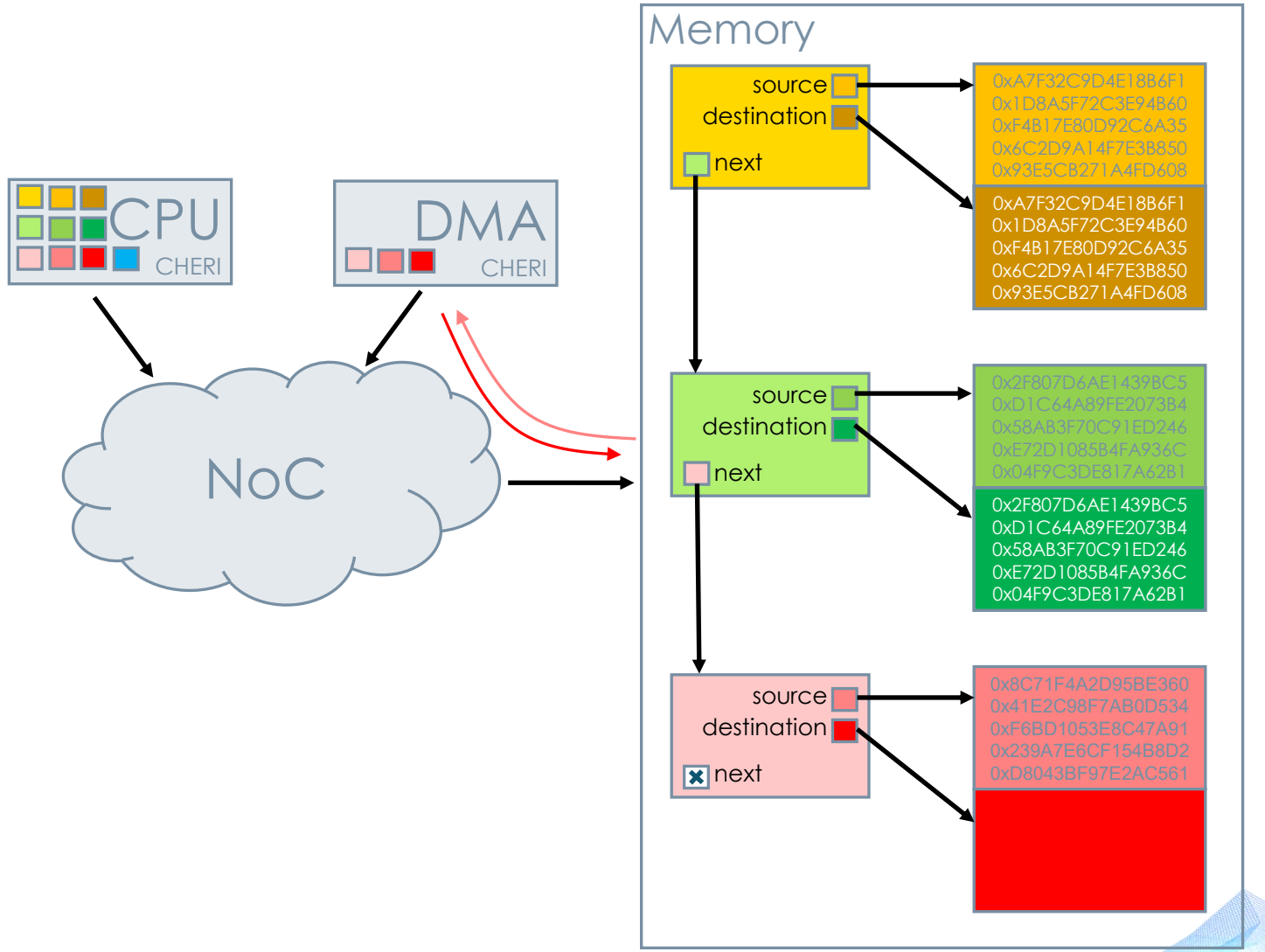
CHERI DMA


Memory
source
destination
next
0xA7F32C9D4E18B6F1
0x1D8A5F72C3E94B60
0xF4B17E80D92C6A35
0x6C2D9A14F7E3B850
0x93E5CB271A4FD608
0xA7F32C9D4E18B6F1
0x1D8A5F72C3E94B60
0xF4B17E80D92C6A35
0x6C2D9A14F7E3B850
0x93E5CB271A4FD608
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0x2F807D6AE1439BC5
0xD1C64A89FE2073B4
0x58AB3F70C91ED246
0xE72D1085B4FA936C
0x04F9C3DE817A62B1
0x2F807D6AE1439BC5
0xD1C64A89FE2073B4
source
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next
0x8C71F4A2D95BE360
0x41E2C98F7AB0D534
0xF6BD1053E8C47A91
0x239A7E6CF154B8D2
0xD8043BF97E2AC561

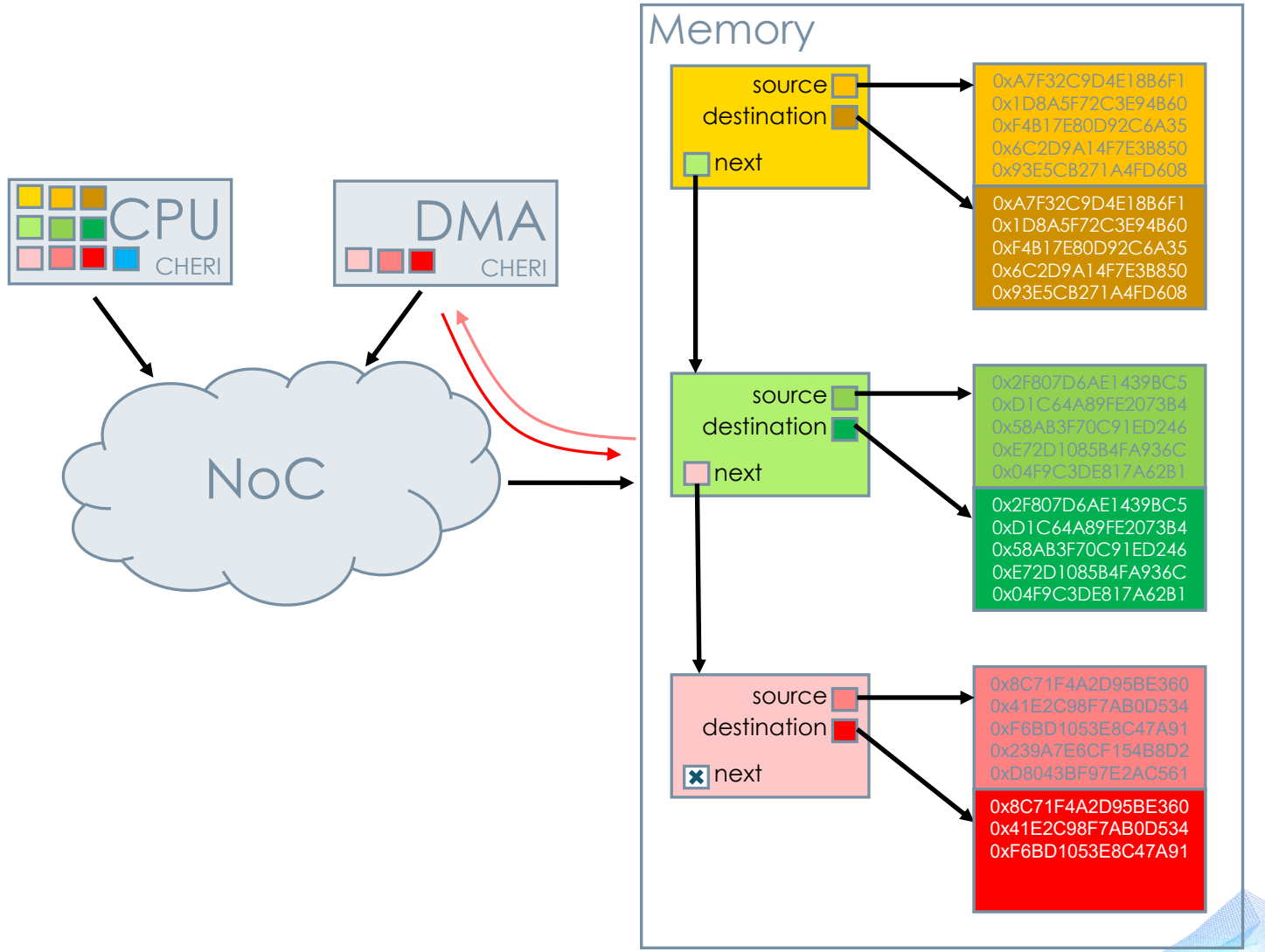
CHERI DMA


Memory
source
destination
next
0xA7F32C9D4E18B6F1
0x1D8A5F72C3E94B60
0xF4B17E80D92C6A35
0x6C2D9A14F7E3B850
0x93E5CB271A4FD608
0xA7F32C9D4E18B6F1
0x1D8A5F72C3E94B60
0xF4B17E80D92C6A35
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0x93E5CB271A4FD608
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0x2F807D6AE1439BC5
0xD1C64A89FE2073B4
0x58AB3F70C91ED246
0xE72D1085B4FA936C
0x04F9C3DE817A62B1
0x2F807D6AE1439BC5
0xD1C64A89FE2073B4
0x58AB3F70C91ED246
0xE72D1085B4FA936C
0x04F9C3DE817A62B1
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0x8C71F4A2D95BE360
0x41E2C98F7AB0D534
0xF6BD1053E8C47A91
0x239A7E6CF154B8D2
0xD8043BF97E2AC561

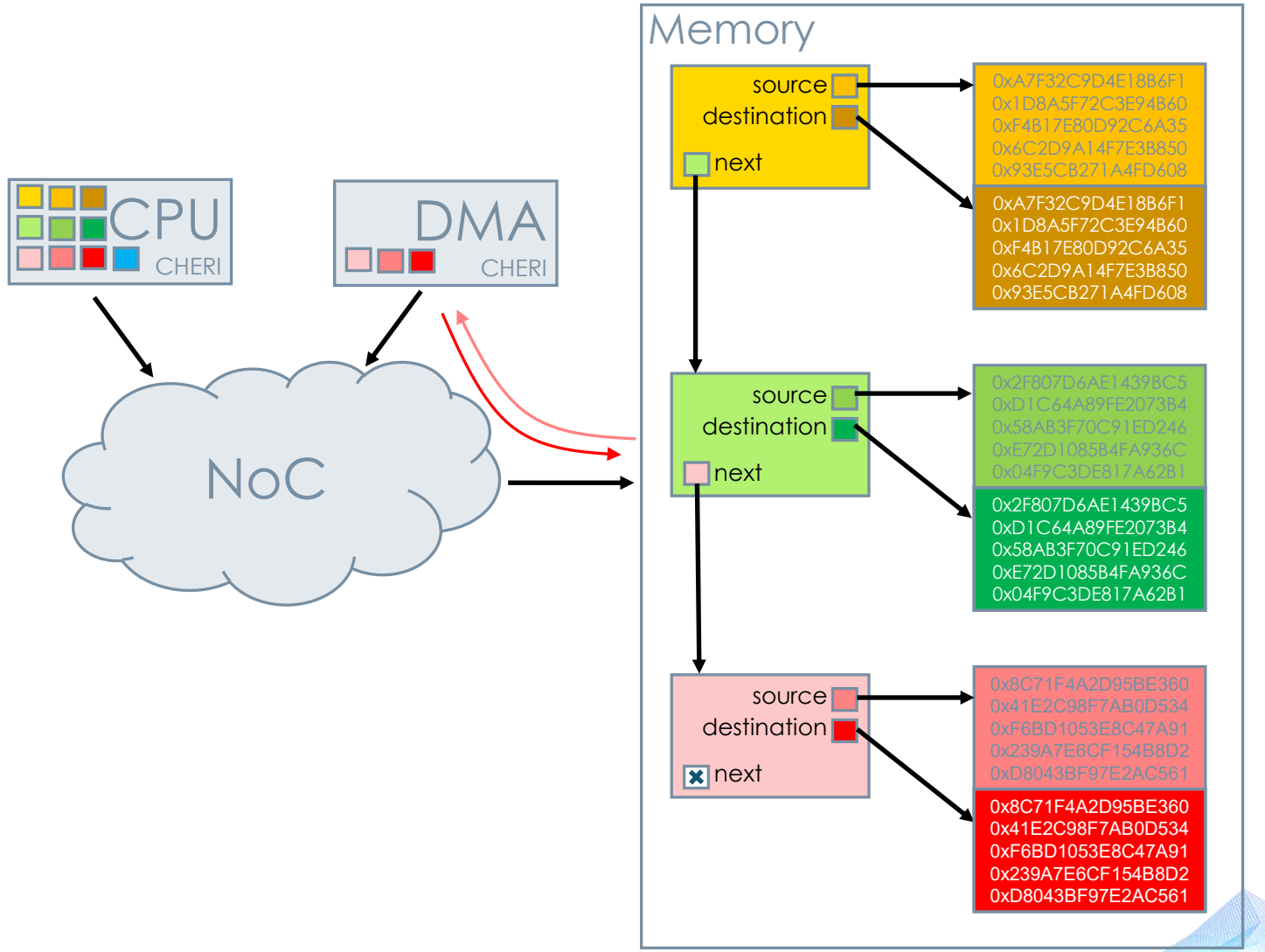
CHERI DMA


Memory
source
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next
0xA7F32C9D4E18B6F1
0x1D8A5F72C3E94B60
0xF4B17E80D92C6A35
0x6C2D9A14F7E3B850
0x93E5CB271A4FD608
0xA7F32C9D4E18B6F1
0x1D8A5F72C3E94B60
0xF4B17E80D92C6A35
0x6C2D9A14F7E3B850
0x93E5CB271A4FD608
CPU
CHERI
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0x2F807D6AE1439BC5
0xD1C64A89FE2073B4
0x58AB3F70C91ED246
0xE72D1085B4FA936C
0x04F9C3DE817A62B1
0x2F807D6AE1439BC5
0xD1C64A89FE2073B4
0x58AB3F70C91ED246
0xE72D1085B4FA936C
0x04F9C3DE817A62B1
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next
0x8C71F4A2D95BE360
0x41E2C98F7AB0D534
0xF6BD1053E8C47A91
0x239A7E6CF154B8D2
0xD8043BF97E2AC561

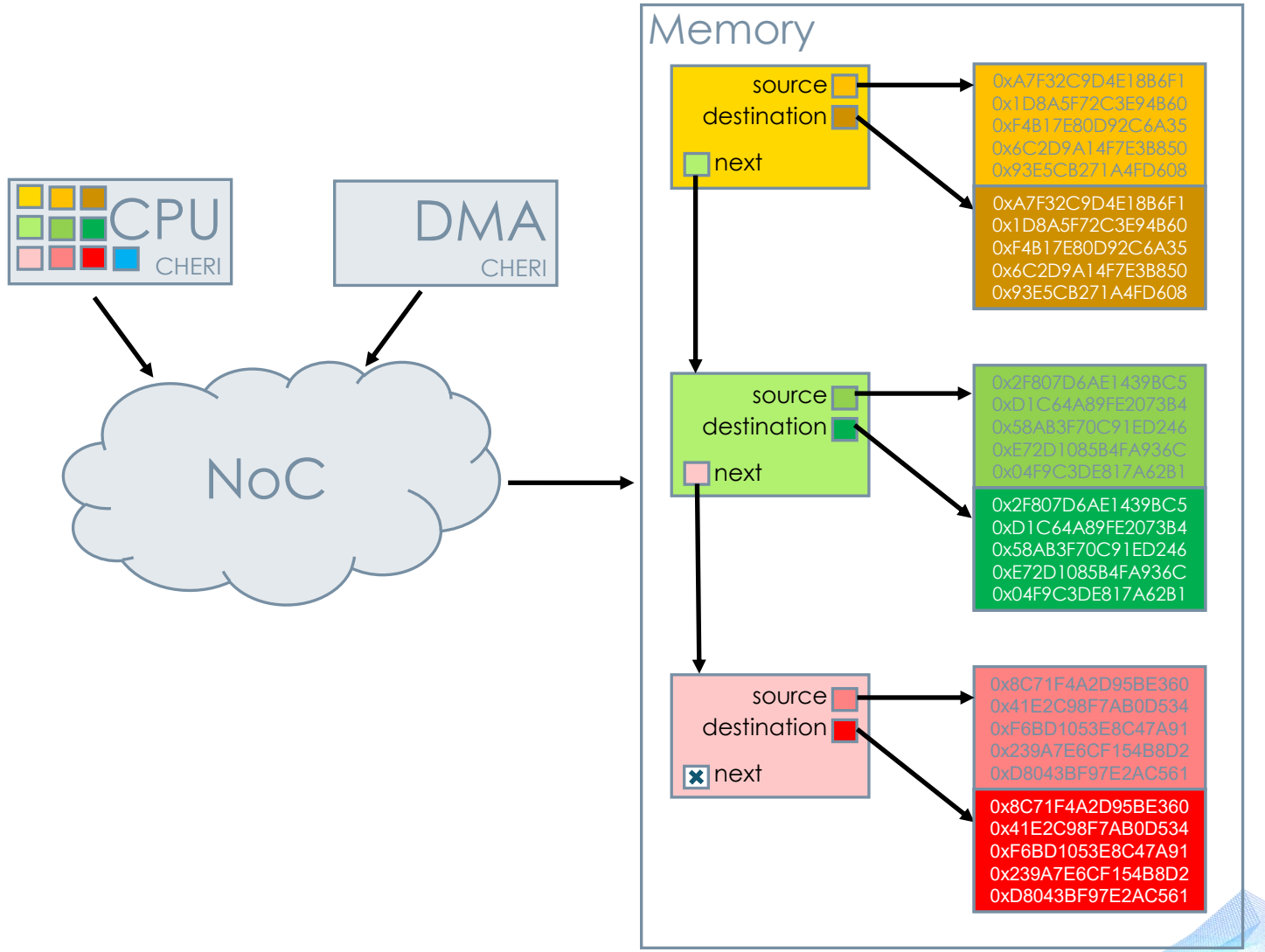
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Memory
source
destination
next
0xA7F32C9D4E18B6F1
0x1D8A5F72C3E94B60
0xF4B17E80D92C6A35
0x6C2D9A14F7E3B850
0x93E5CB271A4FD608
0xA7F32C9D4E18B6F1
0x1D8A5F72C3E94B60
0xF4B17E80D92C6A35
0x6C2D9A14F7E3B850
0x93E5CB271A4FD608
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0x2F807D6AE1439BC5
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0x58AB3F70C91ED246
0xE72D1085B4FA936C
0x04F9C3DE817A62B1
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0x8C71F4A2D95BE360
0x41E2C98F7AB0D534
0xF6BD1053E8C47A91
0x239A7E6CF154B8D2
0xD8043BF97E2AC561
0x8C71F4A2D95BE360
0x41E2C98F7AB0D534
0xF6BD1053E8C47A91

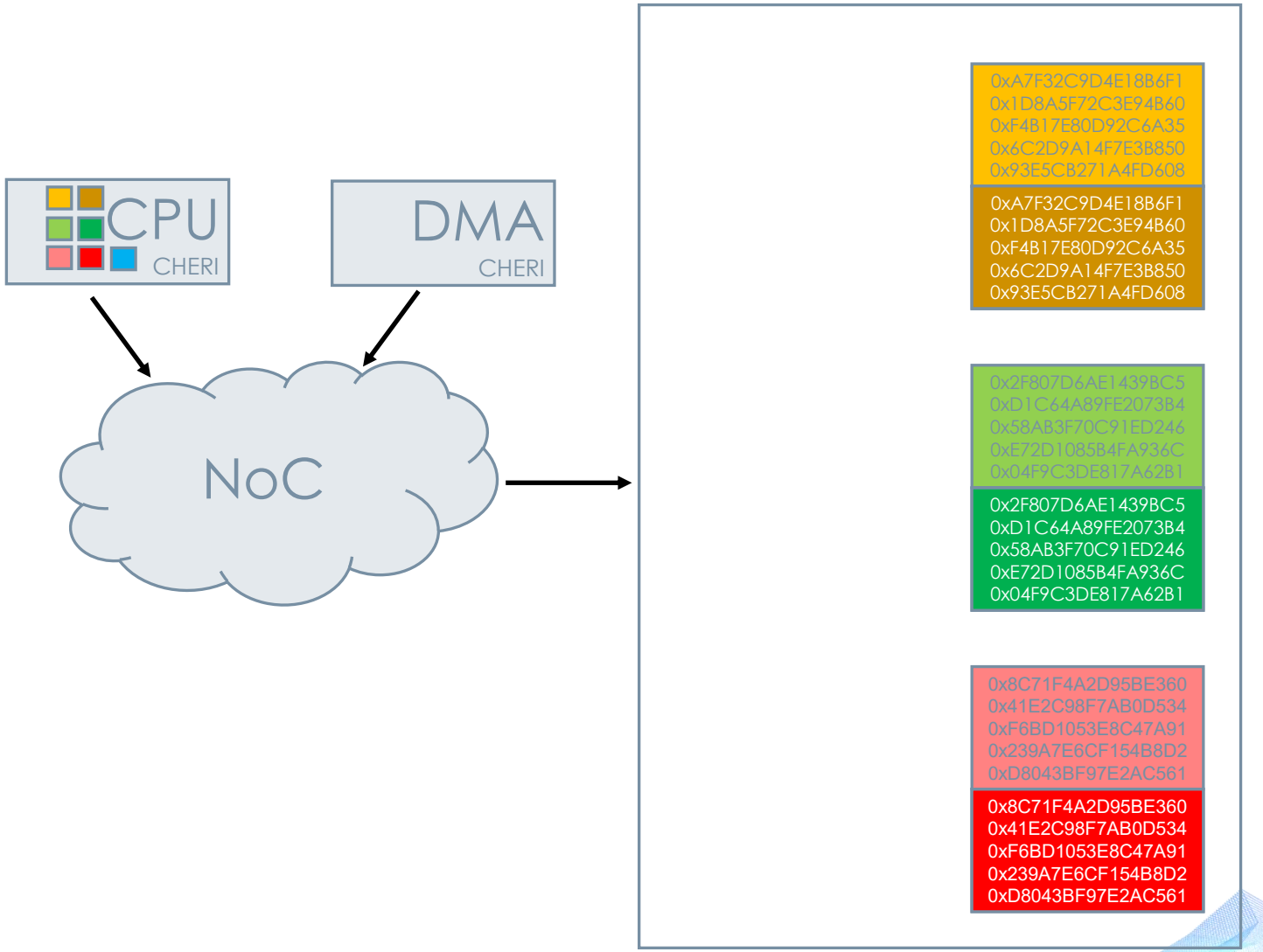
CHERI DMA


Memory
source
destination
next
0xA7F32C9D4E18B6F1
0x1D8A5F72C3E94B60
0xF4B17E80D92C6A35
0x6C2D9A14F7E3B850
0x93E5CB271A4FD608
0xA7F32C9D4E18B6F1
0x1D8A5F72C3E94B60
0xF4B17E80D92C6A35
0x6C2D9A14F7E3B850
0x93E5CB271A4FD608
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0x2F807D6AE1439BC5
0xD1C64A89FE2073B4
0x58AB3F70C91ED246
0xE72D1085B4FA936C
0x04F9C3DE817A62B1
0x2F807D6AE1439BC5
0xD1C64A89FE2073B4
0x58AB3F70C91ED246
0xE72D1085B4FA936C
0x04F9C3DE817A62B1
source
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0x8C71F4A2D95BE360
0x41E2C98F7AB0D534
0xF6BD1053E8C47A91
0x239A7E6CF154B8D2
0xD8043BF97E2AC561
0x8C71F4A2D95BE360
0x41E2C98F7AB0D534
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0xA7F32C9D4E18B6F1
0x1D8A5F72C3E94B60
0xF4B17E80D92C6A35
0x6C2D9A14F7E3B850
0x93E5CB271A4FD608
0xA7F32C9D4E18B6F1
0x1D8A5F72C3E94B60
0xF4B17E80D92C6A35
0x6C2D9A14F7E3B850
0x93E5CB271A4FD608
source
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next
0x2F807D6AE1439BC5
0xD1C64A89FE2073B4
0x58AB3F70C91ED246
0xE72D1085B4FA936C
0x04F9C3DE817A62B1
0x2F807D6AE1439BC5
0xD1C64A89FE2073B4
0x58AB3F70C91ED246
0xE72D1085B4FA936C
0x04F9C3DE817A62B1
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next
0x8C71F4A2D95BE360
0x41E2C98F7AB0D534
0xF6BD1053E8C47A91
0x239A7E6CF154B8D2
0xD8043BF97E2AC561
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0x41E2C98F7AB0D534
0xF6BD1053E8C47A91
0x239A7E6CF154B8D2
0xD8043BF97E2AC561

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0xA7F32C9D4E18B6F1
0x1D8A5F72C3E94B60
0xF4B17E80D92C6A35
0x6C2D9A14F7E3B850
0x93E5CB271A4FD608
0xA7F32C9D4E18B6F1
0x1D8A5F72C3E94B60
0xF4B17E80D92C6A35
0x6C2D9A14F7E3B850
0x93E5CB271A4FD608
0x2F807D6AE1439BC5
0xD1C64A89FE2073B4
0x58AB3F70C91ED246
0xE72D1085B4FA936C
0x04F9C3DE817A62B1
0x2F807D6AE1439BC5
0xD1C64A89FE2073B4
0x58AB3F70C91ED246
0xE72D1085B4FA936C
0x04F9C3DE817A62B1
0x8C71F4A2D95BE360
0x41E2C98F7AB0D534
0xF6BD1053E8C47A91
0x239A7E6CF154B8D2
0xD8043BF97E2AC561
0x8C71F4A2D95BE360
0x41E2C98F7AB0D534
0xF6BD1053E8C47A91
0x239A7E6CF154B8D2
0xD8043BF97E2AC561

Putting this into practice



Codasip is actively developing a CHERI DMA.

- CHERI baked in from the ground up.
- Supports both simple and descriptor based operation.
- Designed to work in environments supporting temporal safety.
- Development is in progress:
  - Initially targets FPGA
  - En route to ASIC-quality IP delivery.

CHERITech'26 CONFERENCE

12–13 Nov 2026
Munich, DE

Located at semi | SEMICON EUROPA

CHERI

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