CHERITech'26
CONFERENCE

CHERI

CHERI Tag Bit Transport Overlay Standard

12-13 Nov 2026
Munich, DE

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IP Director @ Codasip
Working Group Lead @ CHERI Alliance



Located at semi | SEMICON EUROPA

Agenda

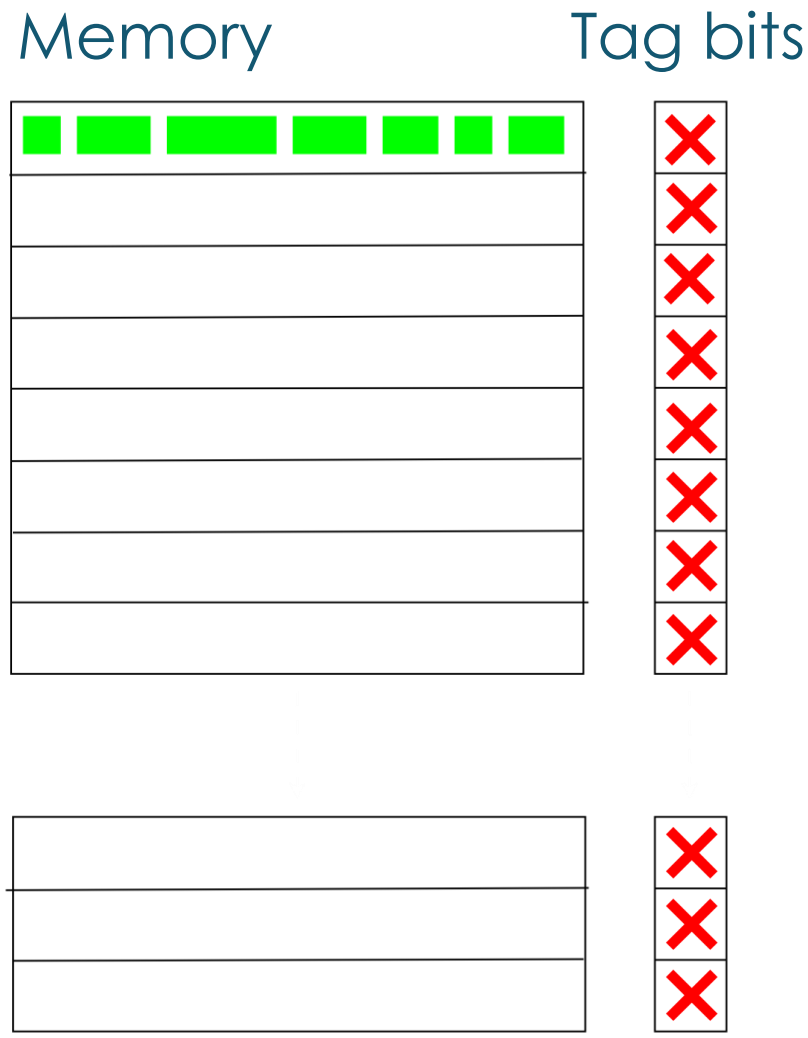
- Why do we need a standard?
- What is the standard about?
- Overview of the standard.
- How you can help develop the standard further.

Why do we need a standard?



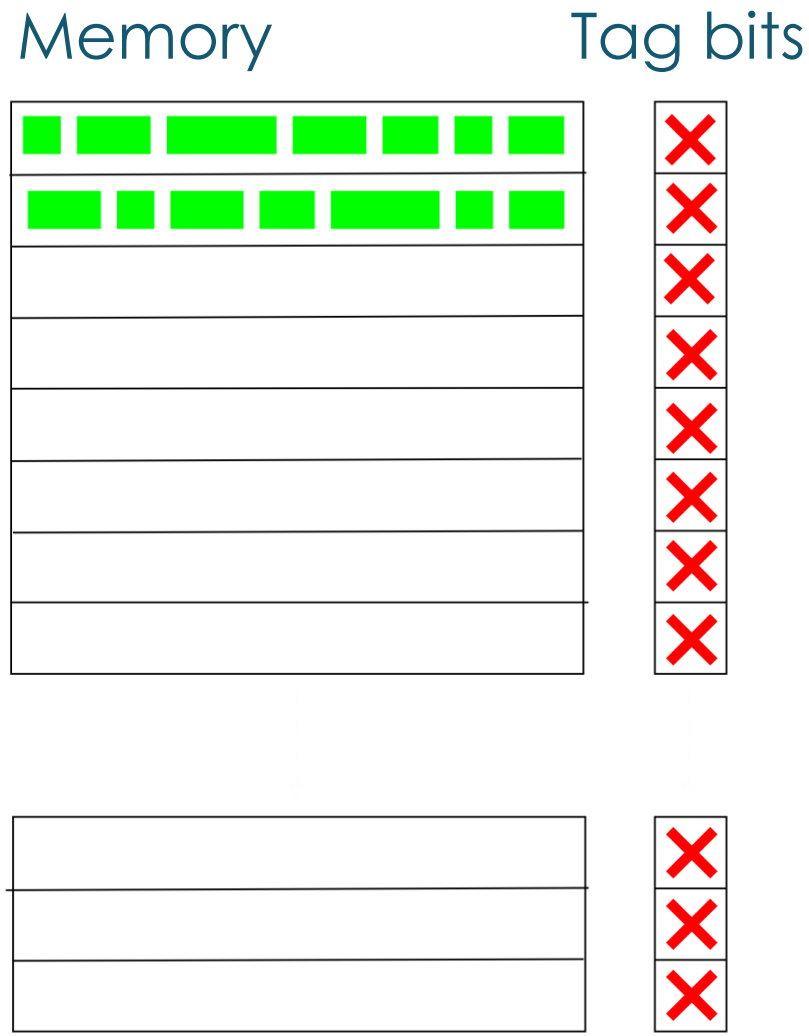
Capabilities and Tag Bits

- Capabilities are made up of both data and a tag bit.
- For every capability sized chunk in memory, there must be an associated tag bit.
- Software cannot directly read or write the tag bits.
- Capabilities only exist where a tag bit is set.



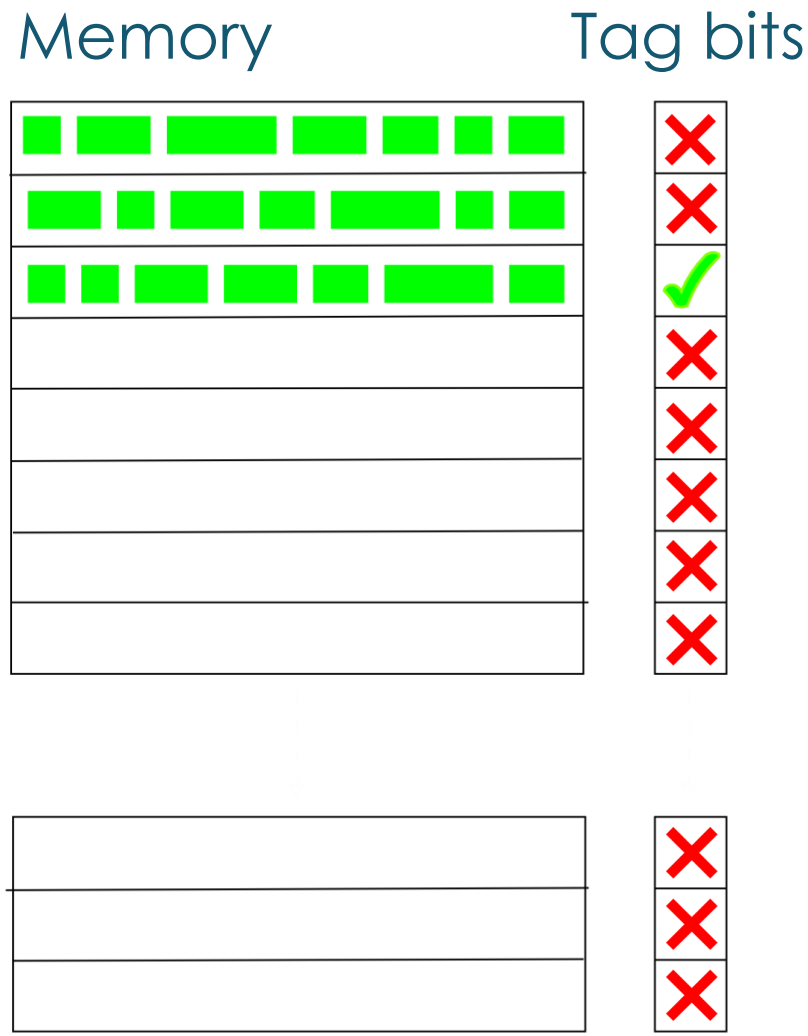
Capabilities and Tag Bits

- If the tag bit is cleared, the data is just plain data.
- Even if the data stores an address within the memory, it cannot be used to access data at that address.



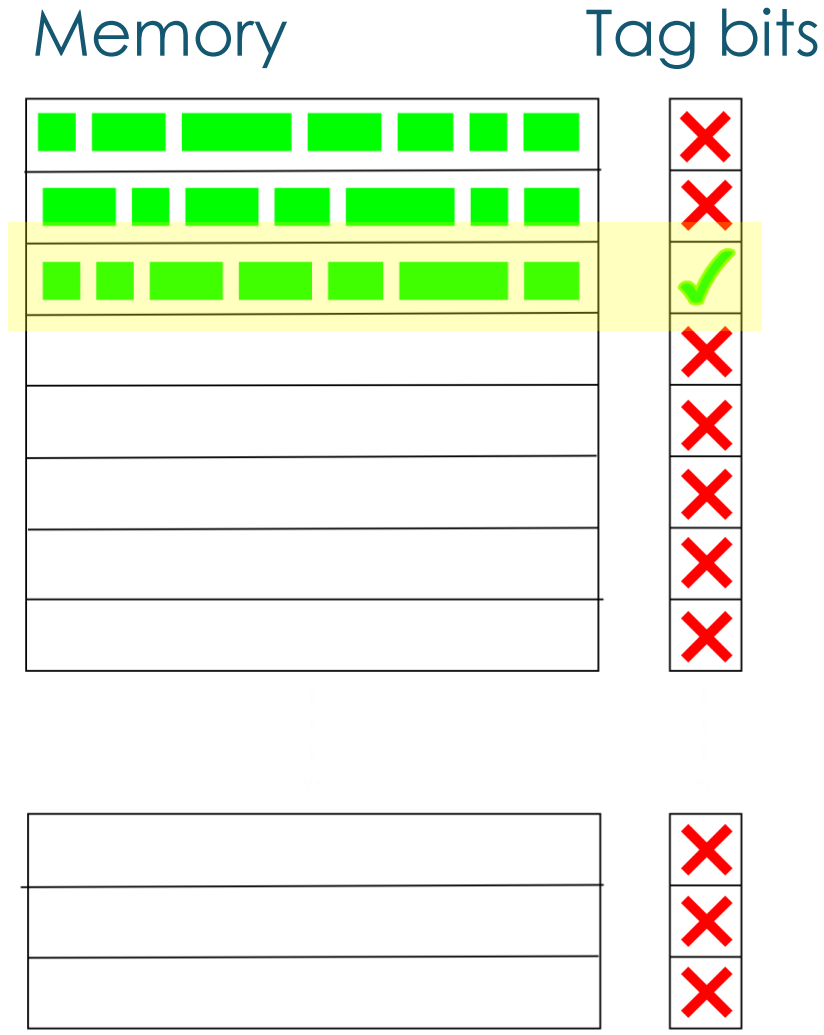
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Capabilities and Tag Bits

- If a tag bit is set, then we have a capability.
- A capability can be used to access memory.
- This standard is all about how we move those capabilities (including the tag bits) around a system.



Why do we need a standard?

- Promote CORRECTNESS in systems implementing CHERI.
- Promote INTEROPERABILITY between CHERI enabled IPs.



What is the standard about?



What is the standard about?

- Provides a set of rules to ensure capabilities are dealt with correctly.
- Provides a set of rules that will promote interoperability between IPs.

Correctness

- Three fundamental rules of CHERI
  - (1) Capabilities are unforgeable.
  - (2) Capabilities are monotonic.
  - (3) Memory can only be accessed using a suitable capability.

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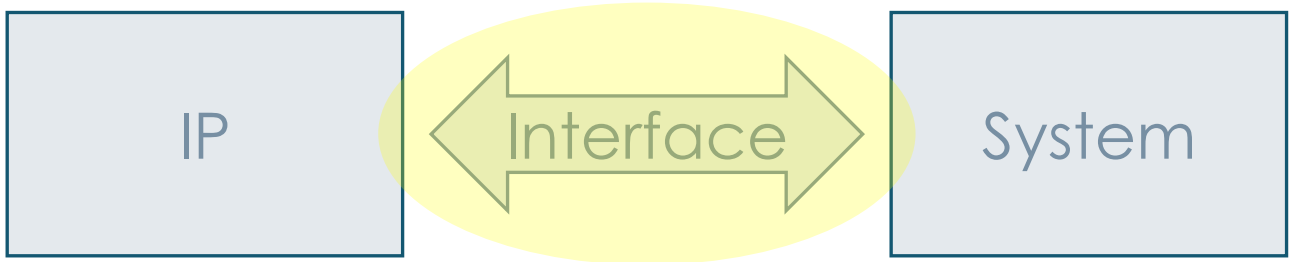
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Interoperability

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- There are many ways of moving capabilities around a system.



Interoperability

- This focuses on the interface
- There are many ways of moving capabilities around a system.
  - How do we make sure that both sides of an interface work properly together?



Interoperability

- Initially the standard specifies how capabilities should be moved via AXI and CHI interfaces (with TileLink to come).

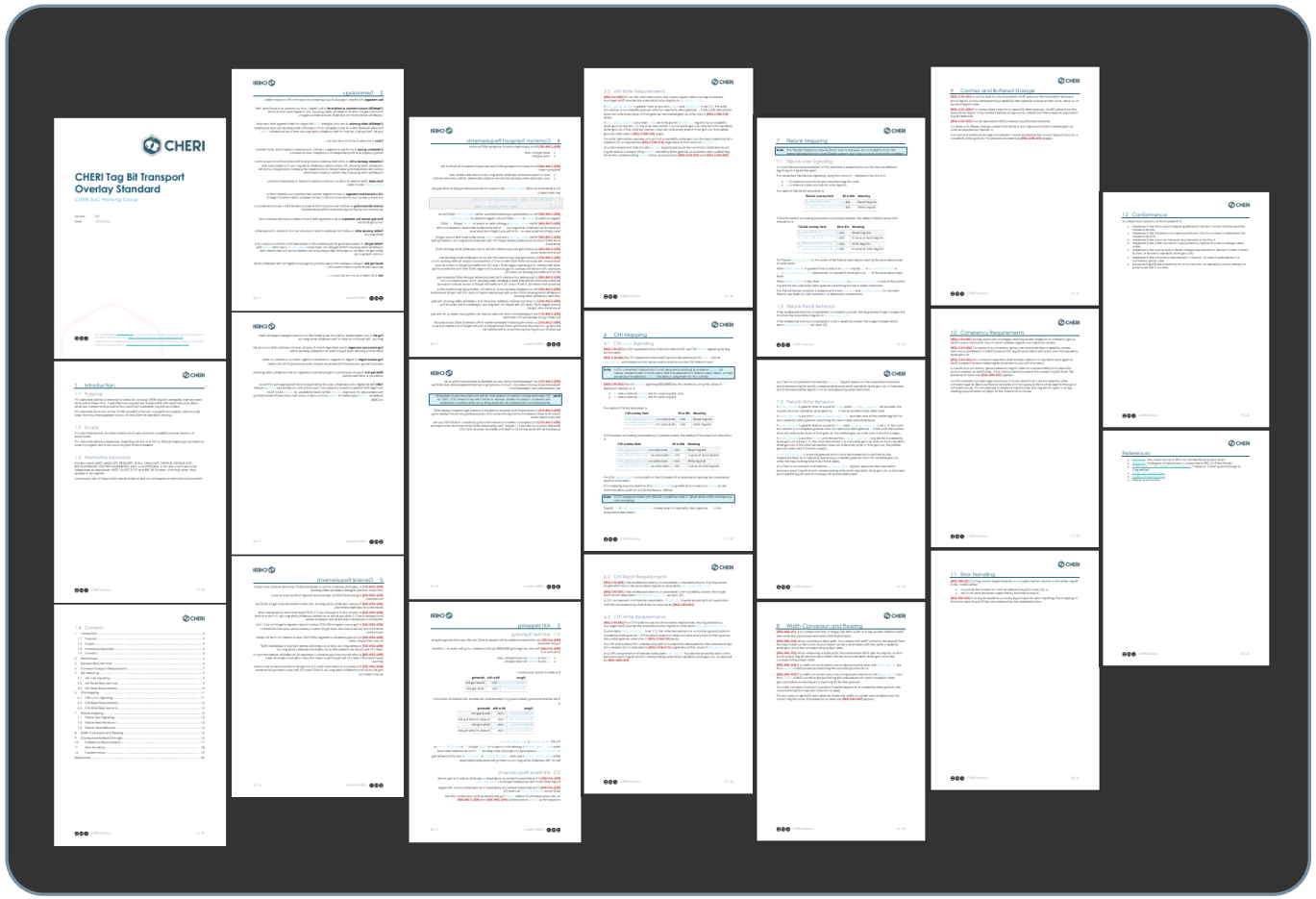


Overview of the standard



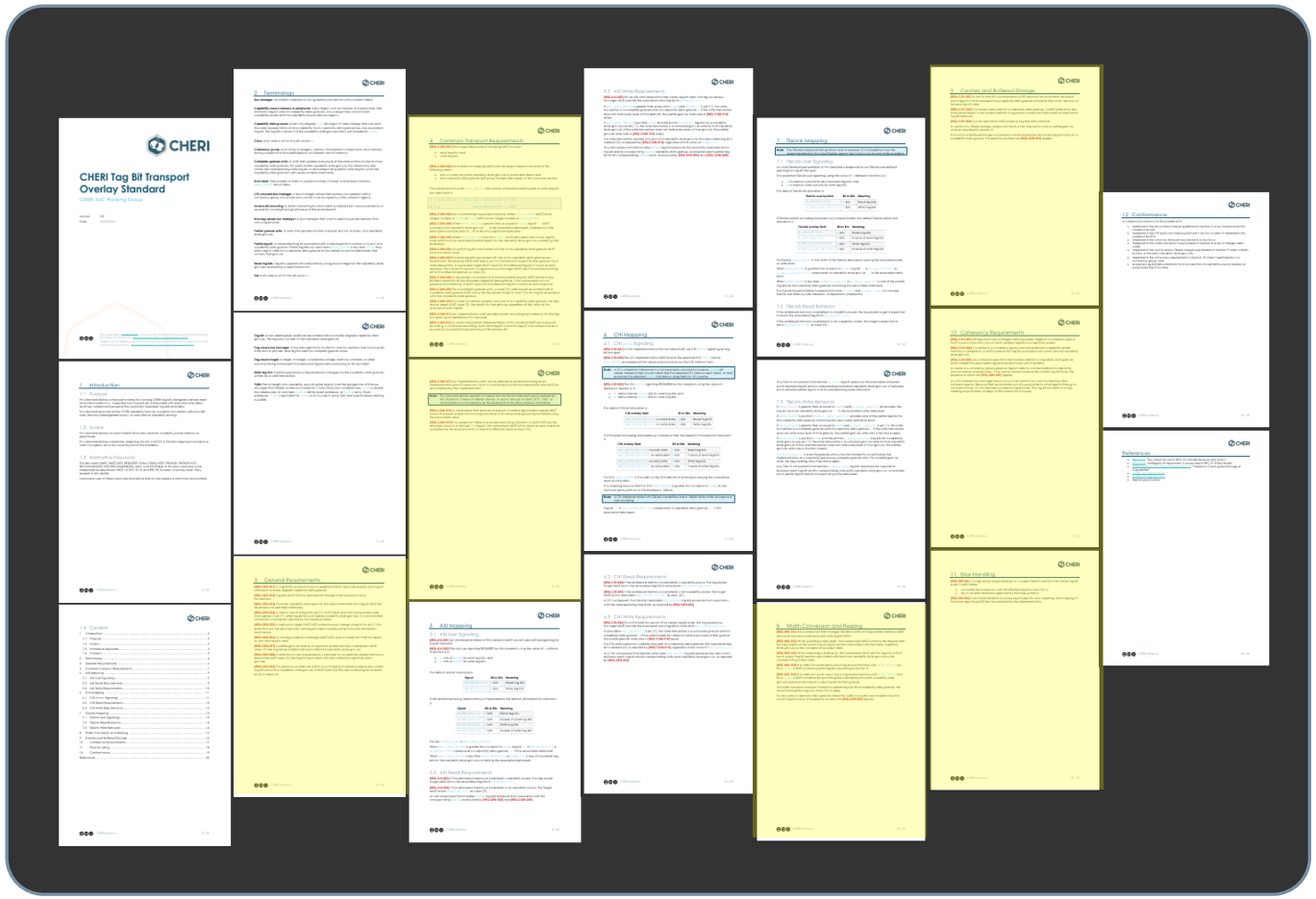
Overview of the standard

- General Requirements
- Common Transport Requirements
- Bus Specific Requirements
  - AXI
  - CHI
  - TileLink (not formalized yet)
- Infrastructure Requirements



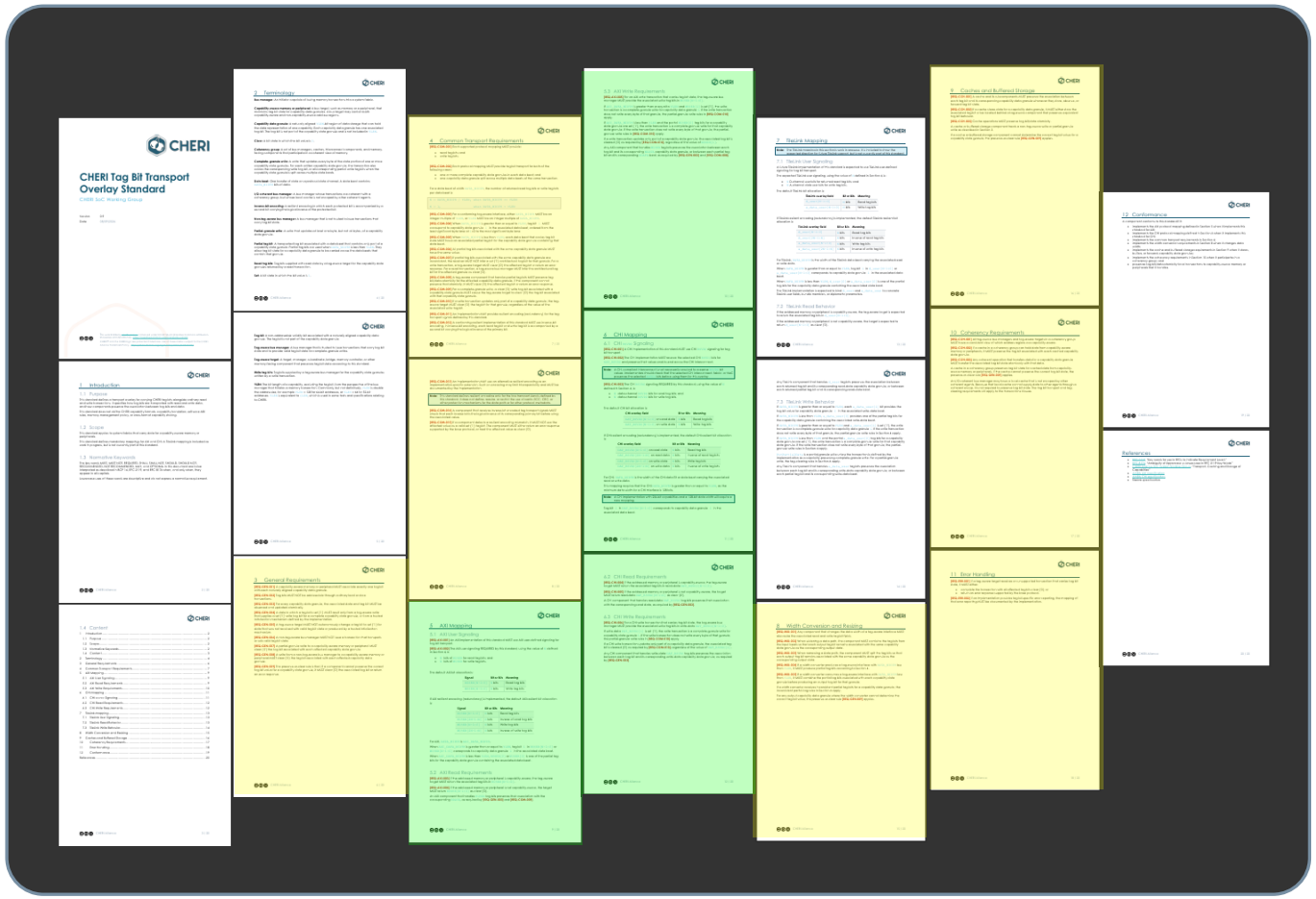
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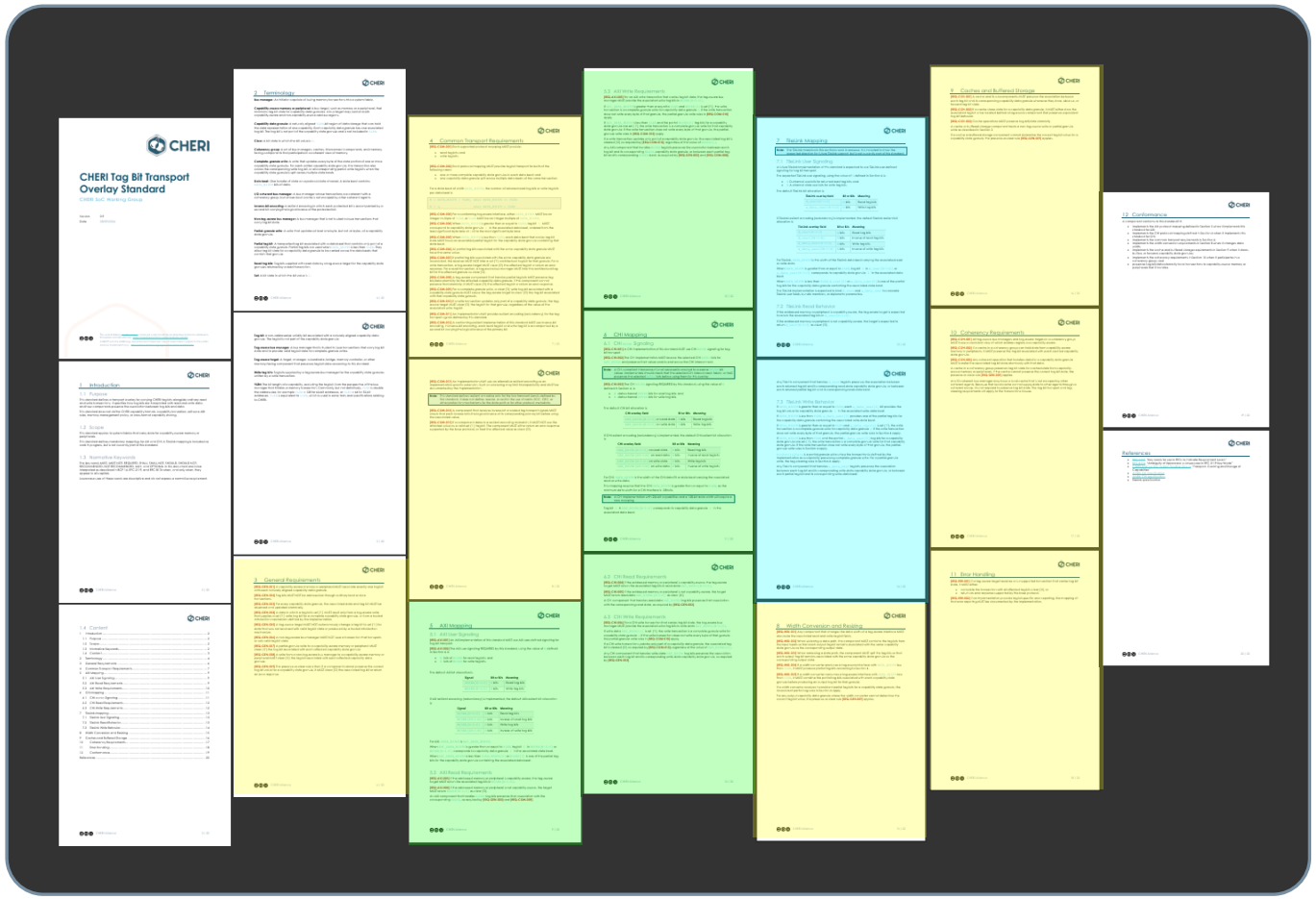
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What kind of rules are in the standard?

- CORRECTNESS Rules:
  - e.g. a rule to ensure that a partial write to a capability will always clear the tag bit (to stop the capability being illegally modified).

> **[REQ-GEN-007]** A partial-granule write to a capability-aware memory or peripheral MUST clear ('0') the tag bit associated with each affected capability data granule.

  - e.g. a rule to stop non-CHERI bus managers creating capabilities.

> **[REQ-GEN-008]** A write from a non-tag-aware bus manager to a capability-aware memory or peripheral MUST clear ('0') the tag bit associated with each affected capability data granule.

What kind of rules are in the standard?

- INTEROPERABILITY Rules:
  - Specific bit mappings for AXI and CHI protocols.
  - Resilient encodings.
  - Rules on how to map wide capabilities to narrow buses.
    - e.g. 128-bit capabilities onto 64-b widths.

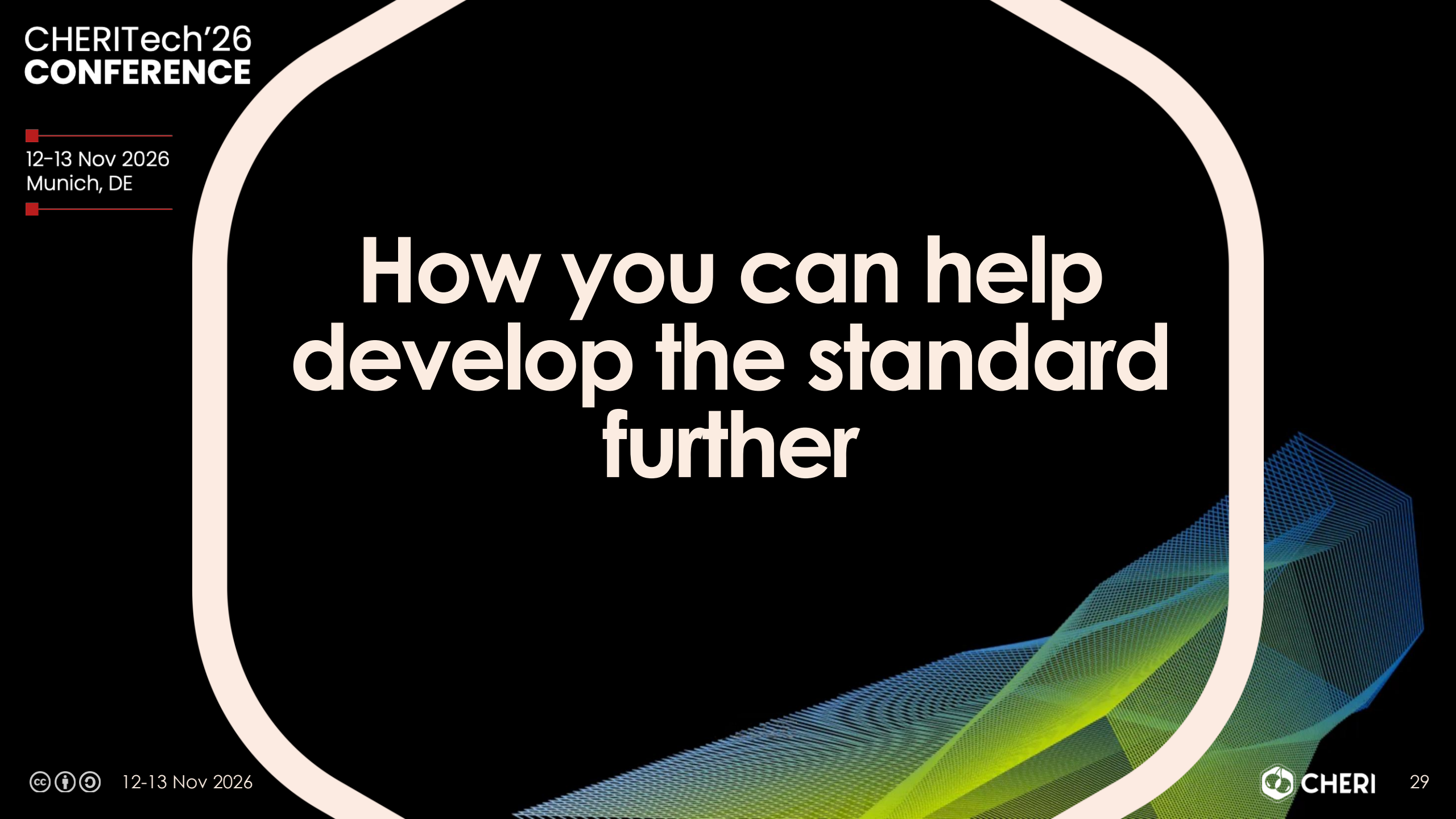
The default AXI bit allocation is:

Signal	Bit or Bits	Meaning
RUSER[N-1:0]	N bits	Read tag bits
WUSER[N-1:0]	N bits	Write tag bits

If AXI resilient encoding (redundancy) is implemented, the default AXI resilient bit allocation is:

Signal	Bit or Bits	Meaning
RUSER[N-1:0]	N bits	Read tag bits
RUSER[2N-1:N]	N bits	Inverse of read tag bits
WUSER[N-1:0]	N bits	Write tag bits
WUSER[2N-1:N]	N bits	Inverse of write tag bits

How you can help develop the standard further



How to help develop the standard.

- Download, read and provide feedback.
  - CHERI-Tag-Bit-Transport-Overlay-Standard-v0.9.pdf
  - We have released version 0.9 for comment.
  - Plan to update to version 1.0 during 2027.

- Join the CHERI-in-SoC Working Group.

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